SESSION E:

IC RADIATION EFFECTS AND HARDENING
ABSTRACT

Total dose irradiation of various CMOS SRAMs is shown to imprint the pattern stored in the memory during irradiation. This imprinted pattern is the preferred state of the memory at subsequent power-up. Imprinting can occur at dose levels significantly below the failure level of the devices and is consistent with the bias dependent radiation induced threshold shifts of the individual transistors of the memory cells. However, before total imprinting occurs, other unusual imprinting phenomena can occur, such as a reverse imprinting effect seen in SOS memories, which is probably related to the bias dependence of back-channel leakage.

INTRODUCTION

Permanent pattern burn-in in CMOS memories from Co-60 irradiation has been previously reported [1]. A transient memory imprint effect has also been reported [2]. Total dose from repeated high dose rate pulses creates a preferred state. The memory can then be triggered to switch to this preferred state, from a complementary state, by a single pulse with a dose rate above the upset threshold. An SEU (Single Event Upset) related imprinting effect has recently been reported [3], where the accumulated dose from high energy proton irradiation creates a preferred state such that the upset probability is reduced and that of the complementary state is increased.

This work reports on an imprinting effect which occurs from total dose accumulation from Co-60 irradiation, but takes place before permanent burn-in. The preferred state does not have to be triggered or observed by additional radiation, but will be the observed state upon subsequent power-up of the memory. When power is first applied to a SRAM (Static Random Access Memory), each memory cell must assume either a one or zero state. If there is sufficient asymmetry in the memory cell such that it always assumes the same state upon power-up, then that cell has a preferred state. Usually, most memory cells have a preferred state, and the preferred state distribution is typically random and about equally divided between ones and zeros across the entire memory. This distribution is changed when a pattern is stored in the memory and the memory is then irradiated.

This effect was first observed while testing a 1K x 1 CMOS/SOI (Silicon-on-Insulator) SRAM. The device was being irradiated with a checkerboard pattern stored in the memory. At various total dose levels the device was removed to perform a complete characterization on an LSIC tester. The device was then returned to the Co-60 cell and the pattern was again stored and the irradiation was continued. After a certain level of total dose was reached, it was no longer necessary to rewrite the pattern after characterization since it came up in that state when power was applied. This led to further study of the effect.

RESULTS

All irradiations were performed in a Co-60 hot cell. With the devices set at the proper distance for the dose rate desired, the source was raised into the room. An ionization chamber probe monitored dose rate and accumulated dose. The devices remained essentially at room temperature.

An initial study compared identical 1K x 1 CMOS SRAM circuits (5μm design rules) fabricated in three different substrate materials (SOS, oxygen implanted SOI, zone-melt recrystallized SOI) using an unhardened process. In this study, a checkerboard pattern was written into the memory and then continuously read during irradiation and checked against the initial pattern. Errors were displayed on a bit map on an oscilloscope as shown in Figure 1. Dose rate was 7 rad(Si)/s. The irradiation was periodically interrupted, power to the memory was cycled off and then on, and the number of errors recorded. Before irradiation, the number of errors after the power off/on cycle for the SOI devices was approximately 50%, in a random pattern, as expected. The SOS devices, however, showed a definite preference for the "1" state. As the total dose increased for the SOI devices, the number of errors at power-up decreased until, finally, no errors would be observed following the power off/on cycle. At this point, the devices were still completely functional and could be written to any other pattern. However, they would return to the imprinted pattern following a power off/on cycle.

The SOS device showed an initial reverse imprinting effect. At a dose of 1 Krad(Si) the device showed 100% errors following the power off/on cycle, indicating that the complementary pattern had been imprinted. As dose increased, the number of errors decreased again and eventually the stored pattern became imprinted as with the SOI devices. The data for all these devices are summarized in Table 1.

Following these initial results on developmental, unhardened devices, attention was turned to both commercial, unhardened devices and to advanced, hardened devices to determine the universality of the effect. To allow a more systematic study, the test procedure was completely automated. A program for a Tektronix 3260 was written to provide a statistical measurement capability. The program applies power to the memory, then reads every location to determine whether it is in a one or zero state. The results are stored and the power is removed. This
cycle is repeated a total of ten times and then is followed by a memory functional test. The functional test consists of six standard patterns (Checkerboard, March, Walk, Galpat 1, Galpat 0, and Galrec). If all six patterns pass, the memory is considered functional. Periodic parametric measurements are also made (access time, high/low output levels, input output leakage, power supply current).

The first devices to be tested with this procedure were non-radiation-hardened 4K x 1 CMOS/bulk SRAMs (Intel 2147). Pre-irradiation tests showed that almost all of the cells had a definite preferred state at power-up. That is, the cell would be either always a one or always a zero (ten out of ten times). The distribution within the SRAM was random, and approximately equally divided between ones and zeros. Less than 5% of the cells showed any degree of indeterminacy, sometimes coming up in a one state and other times coming up in a zero state. Even within this small group, most would show a preference to either a one or a zero, coming up in that state more often than the other, consistently, for many repetitions of the ten cycle test.

Three different irradiation sequences on five devices each were performed. Dose rates were constant for each sequence, but varied from 3.7 to 5.7 rad(Si)/s between sequences. The irradiation was performed in 1 Krad(Si) increments and the test procedure discussed above was performed after each increment. The test sequence involved less than 15 minutes between radiation increments.

The first group of devices had an alternating pattern stored during irradiation. The results of this irradiation sequence are shown in Figure 2.

Imprinting has begun after the first 1 Krad (Si) step. The effect increases with total dose and the pattern is imprinted almost 100% by 6 Krad(Si), which is the failure threshold of the device (output low out of spec). The other two groups of devices had either an all ones or an all zeros pattern stored during irradiation, and gave similar results.

The next group of devices studied involved developmental, radiation-hardened VHSGIC I-like, 1K CMOS SRAMs from three different manufacturers. Tests were performed on four CMOS/SOS devices and five each of two different CMOS/bulk devices. They all basically used a standard six transistor memory cell, except that one of the two bulk types (Bulk-B) included cross-coupled resistors for SEE protection, and the SOS devices included capacitive elements for a similar purpose. The failure level for the SOS devices was 1.6 Mrad (Si). The Bulk-A devices were still functional at 1.6 Mrad (Si) and were not tested at higher doses. The Bulk-B devices showed no failures up to levels as high as 5 Mrad(Si).

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Figure 2. Radiation induced imprinting effect for five identical unhardened 4K x 1 CMOS/bulk SRAMs. The graph shows the results of reading the memory after a power off/on cycle a total of ten times. It gives the percentage of addresses coming up in the pattern that was stored in the memory during irradiation as a function of accumulated dose.

Irradiations were carried out with an alternating pattern stored in the memories, up to a total dose of 1.6 Mrad(Si). Dose increments varied from 1 Krad(Si) for the first increment, to 200 Krad(Si) for the final increments. Dose rates varied from 15 rad(Si)/s for the smallest increments, to 200 rad(Si)/s for the larger increments. Different part types were mixed in each of four different irradiation sequences. The results are shown in Figure 3.

The results for the Bulk-A devices are the simplest, showing imprinting beginning above 100 Krad(Si) and being complete at 350 Krad(Si). The Bulk-B devices show imprinting beginning above 1 Krad(Si) and being complete at 50 Krad(Si). However, upon further irradiation, these devices show a reversal to less than 100% imprinting above 100 Krad(Si) and a return to complete imprinting at 500 Krad(Si). The SOS devices show an unusual reverse imprinting effect, similar to what was observed in the unhardened SOS devices in our initial study as discussed above. This reverse imprinting begins with the first 1 Krad(Si) increment. At 5 Krad(Si), no cells match the stored pattern, while almost 60% of the memory cells match the complementary pattern, as shown in Figure 4. The other 40% of the cells are indeterminate. Above 100 Krad(Si), the stored pattern begins to be imprinted, and is almost completely imprinted at the failure level of 1.6 Mrad(Si).
Figure 3. Radiation induced imprinting effect, as in Figure 2, but for radiation hardened CMOS/SOS and CMOS/bulk SRAMs. The CMOS/SOS devices show an initial reverse imprinting effect.

Figure 4. Imprinting data for the same devices as in Figure 3, but showing the percentage of memory cells matching the complementary pattern to that which was stored during irradiation.

DISCUSSION

A typical six transistor CMOS memory cell is shown in Figure 5.

The stable state for such a configuration is either P1, N2 on and P2, N1 off, or P2, N1 on and P1, N2 off, which are the "one" and "zero" states of the memory cell. At power-up, nodes 1 and 2 will initially assume a value somewhere between Vcc and ground. If all transistors were exactly matched, one could not predict which state the cell would assume. Our data show that, with the exception of the hardened SOS parts, there is sufficient asymmetry in most cells that they always move toward the same state. For example, if the N-channel transistors are dominant, and if N1 is turned on harder than N2 for the same gate voltage, this will pull node 2 lower which will tend to turn N2 off and P2 on. Thus, in turn, pulls node 1 high, turning N1 on harder and P1 off. Thus, the cell would assume the stable configuration of N1, P2 on and N2, P1 off, with node 1 at Vcc and node 2 at ground.

Radiation will shift the thresholds of the various transistors and it is well known that the bias state of the transistor during irradiation affects the magnitude of this threshold shift [4]. The bias state has a larger effect on the N-channel transistors than on the P-channel transistors. The threshold shift for an N-channel transistor will be larger for the transistor biased on (positive gate voltage) due to holes being attracted to the Si/oxide interface, than for the transistor biased off (zero gate voltage). Conversely for P-channel transistors, the threshold shift will be somewhat smaller for the transistor biased on (negative gate voltage) due to holes being pulled away from the Si/oxide interface, than for the transistor biased off (zero gate voltage).

N-channel thresholds initially shift to less positive values due to trapped holes, but with increasing dose, may turn around and shift back to more positive values due to interface state generation. P-channel thresholds shift monotonically to more negative values due to trapped holes. Interface states are not as significant for P-channel transistors since the absence of positive bias inhibits interface state generation, and any interface states would be below the Fermi level, and thus unfilled, at inversion.

For the CMOS memory cell, then, radiation will tend to turn on N-channel devices initially and to turn off P-channel devices. Due to the bias effects noted above, the larger effect for the N-channel transistors will be to reinforce the on N-channel transistor rather than countering the on P-channel transistor. Thus, in both cases, the radiation should tend to reinforce the state that the memory cell is in during the irradiation, and will shift the cell toward a preference for that state at subsequent power-up. Therefore, the ultimate imprinting of the stored pattern during irradiation is what one would expect. This is what is observed for the unhardened SOS and bulk devices and the Bulk-A devices discussed above.

The explanation for the behavior of the hardened Bulk-B devices and the SOS devices is less obvious. A possible explanation for the behavior of the Bulk-B devices is as follows. If the N-channel transistors are initially dominant, the N-channel threshold shifts could fairly rapidly produce complete imprinting. If after this point, the P-channel transistors became dominant, one could see a reduction of the imprinting effect if the P-channel transistors had not yet become fully imprinted. This would not be unusual since the P-channel transistors and the cells would return to 100% imprinting. This is only speculation, and a detailed study of the radiation induced threshold shifts of the individual transistors would be needed to confirm this.
The reverse imprinting effect observed at low dose in SOS memories is most likely due to the bias dependence of radiation induced back-channel leakage in the N-channel transistors. Though radiation induced back-channel leakage is influenced by both gate and drain bias, the drain bias induced fields cause the greater impact on charge trapping in the sapphire substrate and the resulting back-channel leakage [5]. Thus the "off" N-channel transistor in an SRAM cell (gate at zero bias and drain at Vcc) will have more radiation induced leakage than the N-channel "on" transistor (gate at Vcc and drain at zero bias). The ratio of leakage currents induced for "off" bias to "on" bias can be very large at low doses. At subsequent power-up, the greater back-channel leakage path of the previously "off" N-channel transistor would tend to pull that drain low, pushing the memory cell to the opposite state to the one it was in during irradiation. At higher doses, where the bias dependence of leakage currents is not as great and leakage currents tend to saturate, the threshold related imprinting of the stored pattern would be expected to dominate. Again, a detailed radiation study of the individual transistors is required to confirm this hypothesis. It is interesting to note, however, that this reverse imprinting effect was only seen in SOS devices and not in SOI devices, probably due to the different charge trapping mechanisms in sapphire from those in silicon dioxide.

CONCLUSIONS

Our results have shown that complete imprinting by total dose irradiation can occur well below the radiation failure threshold of CMOS SRAMs and that unusual imprinting phenomena can occur at much lower doses than that. These phenomena include the reverse imprinting effect in CMOS/SOS devices. The ultimate imprinting of the stored pattern is consistent with what one would expect from the bias dependent threshold shifts of the individual transistors of the memory cell. One can also argue that the different imprinting behavior observed in different devices, at doses below that required for complete imprinting, are also consistent with the bias dependence of radiation induced threshold shifts and leakage currents. However, a detailed study of the radiation behavior of the individual transistors will have to be done to see if one can simulate all of these phenomena.

Further study is also required to determine the full implications of these effects on radiation test procedures for CMOS memories.

REFERENCES


