Abstract

Focused electron-beam pulses have been used to study and compare collection of ionization generated charge by the gate and induced drain current in GaAs field-effect transistors. Results indicate that hole collection by the gate occurs principally by diffusion, and that built-in fields at the channel-substrate junction inhibit this collection except at the device edges where the gate directly contacts the semi-insulating substrate. At sufficiently high excitation levels the induced drain current is dominated by photoconduction through the substrate from source to drain, and is enhanced by inherent photocooperative gain. The large magnitude of the drain current response relative to the gate collection suggests that it is an important effect for single-particle events in GaAs devices.

Introduction

Measurements of charge collection from alpha particles by devices on semi-insulating (SI) GaAs have been presented in several papers. [1-3] These reports dealt with collection by Schottky barriers or p-n junctions, and the following observations were made: Reference [1] concluded that funneling is apparently not important in SI GaAs, although charge collected within an interval ~2 nsec exceeded what was expected for drift plus diffusion. Data in References [2] and [3] were not time resolved, but both described a significant increase in effective collection depth by Schottky gates at the edge of field-effect transistors (FETs) where the gate overlaps onto the SI substrate. Reference [3] noted that even in the central region of the device the effective collection depth was much greater than the gate depletion depth, with the excess attributed to diffusion and/or bias assisted drift.

In this work focused 39 KeV electron-beam pulses are used to study the time, position, and intensity dependences of charge collection by the gate and of ionization induced drain current in Rockwell FETs. Observed charge collection by the gate is similar to that reported for alpha particles. The data are consistent with ambipolar diffusion as the principal collection mechanism. The effect of the channel-substrate junction in inhibiting diffusion of holes from the substrate to the gate is inferred from data on collection efficiency versus beam location, ionization intensity, and gate bias.

The induced drain response observed for high-level pulses is about 8 times larger than would be obtained by simply collecting generated charge. Although the time dependence approximates that for the gate collection current, these differences are seen: (1) the drain response is uniform in the channel region of the device with no increase at the device edges, and (2) under normal bias the drain response exceeds the gate response in the central channel region by a factor of ~40. Data as a function of ionization intensity implies that the gain occurs when the generated carrier concentration is large enough to induce injected electron current flow through the substrate from source to drain, while at low levels the injection process is blocked by built-in fields at the channel-substrate junction. The mechanism for the high-level gain phenomenon will be discussed. A complementary effect, photovolatic modulation of the channel-substrate junction, has been previously described. [4] The significance of these results for single event upset in GaAs circuits will be considered.

Experimental

The excitation source used for the experiments described is provided by a scanning electron microscope equipped with electrostatic beam-blanking as described in Reference [4]. At 39 KeV an electron-beam penetrates ~4.5 µm into GaAs. [5] A normalized, integrated dose rate versus depth curve is shown in Fig. 1. For an electron-beam current of 10 nA the charge generation rate is approximately 25 fC/µm per nsec for the initial 2 µm of penetration depth. At the surface the beam is focused to <10 nm radius, but it widens with depth due to scattering with the maximum diameter of the generation volume being comparable to the penetration depth. [6] By comparison, an alpha particle deposits ~8 fC/µm in a period <<1 nsec. The initial radius of the ionization track is <<1 µm, but it widens on a nanosecond timescale due to ambipolar diffusion. The virtually instantaneous deposition and initial very high ionization density have at least two important consequences: (1) the possibility of charge funneling, and (2) drift current spikes in high field regions with time scales <<1 nsec. As noted in Reference [1], charge funneling may not be an important effect in SI GaAs. Subnanosecond drift current spikes from charge deposited in the depletion region of the gate are expected, and one of the purposes of these experiments is to evaluate the relative importance of subnanosecond drift collection versus other charge collection and induced current effects which are observed.

The principal limitation of electron-beam pulse experiments for studying single event phenomena is the inability to produce an initial very high density track in which funneling might occur. The deposition interval can be reduced to about 250 psec using optimal beam-blanking equipment. Although this is still slow compared to high energy ion events, it may approach circuit or device response time. The advantages of electron-beam pulses are: (1) The location and depth of excitation can be easily controlled. (2) Repetitive pulses can be applied to allow use of sampling techniques and signal averaging. (3) The beam intensity is variable, and can be made >1 pC/nsec per µm of penetration. (4) The equipment required is relatively economical to acquire and operate. In view of these trade-offs, focused electron-beam pulse experiments appear useful as a supplement to other experimental approaches. Data are presented for Rockwell FETs fabricated on nominally undoped SI GaAs. The gate length is 1 µm and the width is 50 µm. The pinch-off voltage is about -1 V.

*Funded by DARPA
Results and Discussion

The effect of the channel-substrate junction is important for interpretation of the results given below. Figure 2 shows a schematic model which illustrates the salient feature of the junction, the space charge region which is formed. The substrate properties are assumed to be dominated by shallow acceptor impurities which are excess of native deep donors. [7] Near the n-channel the deep donors are neutralized and a space charge of locally uncompensated acceptors remains. Some properties of the junction, which are mainly determined by the shallow acceptor concentration, can be inferred from photovoltaic channel modulation experiments as described in Reference [4]. It is interesting to note that although nominally undoped SI GaAs typically exhibits weak n-type conductivity, the channel-substrate junction is not an n+-n-

"high-low" transition, but rather is more similar to a one-sided n-p junction. The presence of the junction has several important consequences. It separates electron-hole pairs with resulting photo-voltaic modulation of the channel. It inhibits gate collection by diffusion of holes from below the channel. It also confines electrons to the n-regions and prevents direct photoconduction through the substrate. All of these effects occur only so long as the excitation level is not large enough that the charge associated with generated free carriers becomes comparable to the space-charge in the junction region. When this occurs the junction "flattens out," the photovoltaic channel modulation effect saturates, inhibition of hole collection is reduced and photocollection of injected carriers through the substrate occurs. Data presented below and in Reference [4] show these phenomena.

Data on gate collection efficiency versus position are shown in Fig. 3. For these measurements the beam generation current is kept relatively small compared to "high-level" data presented below. The beam is operated in a DC mode rather than pulsed, and the current which flows into the gate is measured as the beam location is scanned across the width of the device as illustrated. The beam is kept between the gate and drain with an aid by the gate metal. For the data of Fig. 3 no drain bias is applied, and hence there is no significant difference between source and drain. In 3(a) no gate bias is applied either, and thus collection occurs due to diffusion and separation of electrons and holes by built-in fields only. The collection efficiency has maxima of about the channel width and extends into the channel, where the gate extends into the SI substrate. The reason for these maxima is that holes below the channel are inhibited from reaching the gate by the channel-substrate junction, except near the edges where they are able to reach the gate directly. Electrons are collected by the n-channel. In 3(b) a bias of -1.5 V is applied to the gate. This bias is sufficiently larger than the pinch-off voltage that the channel is completely depleted and the effect of the substrate junction field is almost eliminated, allowing effective hole collection across the width of the device. Figure 4 shows data similar to Fig. 3, but from a more accurate measurement. For zero bias the maximum effective collection depth at the edge is ~2 μm, and in the center it is ~0.1 μm. The first value is consistent with collection by diffusion with an ambipolar diffusion length of ~2 μm, [5] while the second value indicates collection of charge generated within the channel only.

The gate collection enhancement at the device edge is dependent on device geometry, excitation intensity, and applied bias fields. At high excitation levels the recombination rate across the substrate junction increases, [4] and the influence of applied bias fields in assisting collection increases while the collection inhibiting effect of the junction decreases. Figure 5 shows high-level gate current line Scan data which in comparison with Fig. 4 illustrates these effects. Such considerations also apply to the observations in Reference [2] regarding collection efficiency versus position and bias for a different geometry device. An alpha particle track would produce a high-level ionization density.

The time dependence of the high-level gate current collection is shown in Fig. 6. Disregarding some bumps which are introduced by the instrumentation, the rise and fall time are estimated to be about 1.5 nsec. This is again consistent with ambipolar diffusion as the principal collection mechanism, although drift certainly contributes since the collection efficiency is bias dependent. A subnanosecond drift component would be expected from the depletion region between the gate and channel, but its magnitude would be limited because the channel depth is much less than the effective collection depth. The relative importance of "prompt" versus diffusion collection for particle events will be considered below.

Figure 7 compares the position dependences of the induced drain response and the gate collection for high-level excitation. Note that the gate response is magnified X10, and that the peak collection efficiency is less than 0.5; while the induced drain current is 4 times larger than the total generation current and ~ 8 times larger than would be expected for collection by diffusion.

Figure 8 compares the dependences on excitation level of the induced drain and gate responses. For these data the gate bias was -1.5 V, so that the channel was strongly depleted. This eliminates the channel modulation and inhibited collection effects as previously noted. The bias drain was 0.75 V. The data show that at low levels the drain and gate together act like a diode with a collection efficiency of about 0.6 as before. At high levels the gate efficiency decreases somewhat, while the photoconductive gain in the drain response is manifested. The generated carrier concentration at which the transition occurs can be estimated: Taking the excitation volume, accounting for generation and diffusion, to be approximately 4 μm in diameter by 6 μm deep and assuming an ambipolar lifetime of 2 nsec, a generation current of 100 μA corresponds to a nonequilibrium carrier concentration of ~2x10^16 cm^-3. This value is comparable to or exceeds expected shallow and deep-level concentrations for SI GaAs. [7] Above this concentration the ionized free carrier charge is dominant in the SI region.

Figure 9 compares the time dependences of the drain and gate responses. Here the gate and drain bias levels of -0.75 and -0.75 V, respectively, give a drain current close to zero, but do not strongly deplete the channel. This would be a normal "off" state for the device. The beam is positioned in the central device region. Note that the gate response is again magnified X10 for comparison. Disregarding spurious bumps as before, the rise and fall time of the induced drain current is about 2 nsec, which is similar to the gate time response. The gain observed in the drain current response is presumably related to that which has been reported for optical excitation, [8] and for a new type of bipolar n-p-n transistor fabricated on SI GaAs. [9] This gain could be interpreted as resulting from the induction of a virtual parasitic bipolar transistor. It is easily understood that for contacts that are
Figure 1. Normalized, integrated dose-rate versus depth for a 39 KV electron-beam incident on GaAs.

Figure 2. Representation of the n-channel to SI substrate junction. See text for explanation.

Figure 3. Gate collection efficiency versus position. The generation current is 2 μA. The gate current to generation current ratio is shown for linescan across the device between the dashed arrows. In (a) no bias is applied. In (b) the gate bias is -1.5 V, which considerably exceeds the pinch-off voltage of about -1 V.

Figure 4. Gate linescan data for low-level generation and various bias conditions. The generation current is 2 μA. The gate and drain biases are: in (a) -1.5 and 0.0 V, in (b) -0.75 and 0.75 V, and in (c) 0.0 and 0.0 V.

Figure 5. Gate linescan data for high-level generation. The generation current is 160 μA. Bias voltages are the same as in Fig. 4.
Figure 6. Time dependence of the gate current response at an edge maximum. The generation current is 800 $\mu$A, the gate bias is -0.75 V, and the drain bias is 0.75 V.

Figure 7. Comparison of the position dependence of the gate collection current and the induced drain current. Note that the gate response is magnified X10 for comparison. The generation current is 160 $\mu$A, the gate bias is -0.75 V, and the drain bias is 0.75 V.

Figure 8. Plot of gate and drain response with the channel strongly depleted (gate bias -1.5 V and drain bias 0.75 V) versus generation current.

close enough and electric fields that are high enough for generated carrier lifetimes to be greater than carrier sweep-out times that a photoconductive gain equal to the electron to hole mobility ratio will result. For Si GaAs this ratio is -10. The observed nanosecond timescale indicates that diffusion also plays a role in the process. We speculate that this is due to diffusion of carriers from the low-field region in the substrate to the high-field region proximate to the device where sweep-out limited photoconductive gain occurs. Two or three dimensional numerical simulation including ambipolar diffusion and substrate junction effects would be desirable to provide quantitative understanding of these phenomena.

Conclusion

The results described above have implications regarding single-event upset mechanisms in GaAs circuits. Consider the following rough estimates. A heavy ion might deposit $\sim$100 fC/µm. After a nanosecond the radius of the excitation volume would be $\sim$1 µm, and the nonequilibrium carrier concentration would be $\sim$$10^{17}$ cm$^{-3}$. The prompt current which would flow from the gate depletion region would be $\sim$10 fC in an RC time constant limited interval on the order of 100 psec. The diffusion current which would flow from the gate would be $\sim$50 fC in an interval of 1 to 3 nsec at the center of the device, or about 200 fC per the interval at the maxima at the device edges. The current which would be induced in the drain would be $\sim$800 fC in the 1 to 3 nsec interval. The drift current spike would have an amplitude of $\sim$100 $\mu$A, the diffusion current amplitudes would range from 20 to 200 $\mu$A, and the induced drain current pulse would be 200 to 800 $\mu$A. The drain current in the 50 $\mu$m wide test device was 2.5 mA at $V_{GS} = 0$ and $V_{DS} = 0.75$ V; however, an
actual IC switching element would likely be much smaller, and thus the estimated current levels could possibly produce upset in GaAs digital logic. We believe that all of the above contributions are potentially important, and should not be neglected in efforts to assess probable upset rates.

Acknowledgements

Sample devices were kindly provided by F. Eisen of Rockwell International, Thousand Oaks. Conversations with A. K. Nedoluha, P. J. McNulty and J. R. Srour are gratefully acknowledged.

References


