The effects of 2 MeV electrons, up to a dose of $10^5$ rad(ZnS), on DC biased and continuously operating (Hg, Cd)Te charge-coupled devices (CCDs) at 77 K are discussed. Radiation induced flatband shifts were observed to be proportional to the electric field in the gate insulator. Typical flatband voltage shifts for thick insulator areas of the device were 3 volts for a dose of $1x10^4$ rad(ZnS). Degradation in CCD performance characteristics was observed in devices which were irradiated during operation. This degradation is attributed to flatband shifts in the interface state density. After $10^4$ rad(ZnS), charge transfer efficiency and 'effective' full well capacity had decreased from pre-irradiation values of .996 and $8x10^{11}$/cm$^2$ to .992 and $4x10^{11}$/cm$^2$, respectively. Charge collected during a 1 msec integration of the dark current had increased by a factor of three from a pre-irradiation value of $1.2x10^{11}$/cm$^2$ to $3.8x10^{11}$/cm$^2$.

**INTRODUCTION**

(Hg,Cd)Te has emerged as the semiconductor material of choice for high performance infrared detectors in the 3-5 and 8-12 micron wavelength atmospheric transmission windows. The success of these devices is due to the large integration (time delay and integration) monolithic (Hg,Cd)Te IIRCCD (Infrared Charge Coupled Device) focal planes which detect radiation in the 3-5 micron wavelength region. These devices have been reported [1]. This represents the most advanced MIS (Metal-Insulator-Semiconductor) device fabricated in this material to date. Typical charge transfer efficiencies ($\eta$) and full well charge capacities ($Q_{FW}$) of these devices are .996 and $5x10^{11}$/cm$^2$, respectively, though $\eta$ and $Q_{FW}$ as large as .9995 and $1x10^{12}$/cm$^2$ have been reported. Low background integration times as long as 1 sec have been observed. It is anticipated that these focal planes will be used in FLIR (Forward Looking Infrared) imagers operating in the scanned mode. The CCD will perform both the IR detection and the TDI which is used to enhance the detector signal to noise ratio.

The effects of ionizing radiation on (Hg,Cd)Te photoconductive and photovoltaic IR detectors has been reported [2,3]. For both kinds of device, performance degradation is dominated by surface and insulating passivation layer effects such as interface state generation and fixed charge buildup. Both of these phenomena would be expected to be important in affecting MIS CCD performance. The effect of ionizing radiation on (Hg, Cd)Te MIS capacitors has been reported [4], but no data has been published on more sophisticated devices such as FETs or CCDs. This work reports for the first time on ionizing radiation effects in (Hg,Cd)Te CCDs. Flatband shifts in (Hg,Cd)Te CCDs which were DC biased during irradiation, and performance degradation in (Hg, Cd)Te CCDs which were operated continuously during irradiation were measured.

Space considerations do not permit a presentation of CCD fundamentals. Instead, the reader is referred to a number of review papers on the subject [5-7]. The state of the art in CCD imagers has been reviewed by Barbe[8], and the effect of ionizing radiation on Si CCDs has been reviewed by Killiany[9]. The effects of ionizing radiation on Si CCDs irradiated at cryogenic temperatures are greater than when the same device is irradiated at room temperature. For example, devices which are radiation hardened for room temperature operation (i.e., $AV_{FB} = -2$V after $10^5$ rad(Si)) still exhibit large (2 volt) flatband shifts at $10^6$ rad (Si) when irradiated at 90 K [10]. In general, it is expected that flatband voltage shift and increased interface state density caused by ionizing radiation will degrade the performance of CCDs by causing a decrease in full well charge capacity and transfer efficiency, and by causing an increase in dark current. Imperfect charge transfer in CCD focal planes results in a degradation in image sharpness as measured by a decrease in the modulation transfer function (MTF) for the device. In order to avoid serious degradation in image quality, it is necessary to have the product of the transfer inefficiency $(1-\eta)$ and the number of transfers less than approximately .1 [11]. Full well charge capacity requirements are precisely determined by imaging system design and scene conditions, but for most applications, a charge capacity of $5x10^{11}$/cm$^2$ is adequate. Insufficient charge storage capacity results in image quality degradation through blooming and loss of dynamic range. Dark current in IRCCDs limits the allowed integration time and usable well capacity and increases the noise. Required integration times again are determined by system design and scene specifics, but for typical applications 1 msec is considered adequate.

**EXPERIMENTAL TECHNIQUES**

The CCDs studied in these experiments are 32 bit, four phase, p-channel shift registers fabricated by Texas Instruments. Cross sectional views of the device are shown in Figures 1 and 2. This structure forms the basic building block for the complete 16x32 focal plane mentioned above. The device uses a dual layer insulator consisting of an anodic oxide and vacuum deposited ZnS layers. The anodic oxide layer is employed to achieve a high quality semiconductor/insulator interface characterized by an interface state density in the $3x10^{10}$/cm$^2$-eV range [12]. The (Hg,Cd)Te is n-type having a carrier concentration in the $5x10^{14}$ to $1x10^{15}$/cm$^3$ density.
range, with a bandgap of approximately 0.28 eV. Charge is confined to the CCD channel by an aluminum MIS field plate. The CCD gates are vacuum deposited nickel approximately 100 angstroms thick and are semitransparent in the 3–5 micrometer wavelength region. Individual gate area is $5 \times 10^{-6}$ cm$^2$. Electrical charge input to the CCD is achieved by pulsing the input gate (IG in Figure 2) in the tunneling regime, and allowing the tunneling generated charge to spill into the adjacent empty potential well [13]. The device is operated in the double well clocking mode with most of the charge stored under the lower level ($\phi_2$ and $\phi_4$) gates [14]. Charge is sensed at the output of the device using a floating gate (FG in Figure 2) which is connected to an off-chip silicon based source-follower circuit. The source-follower output is further amplified by a low noise X8 preamplifier, and then fed to a correlated double sampling circuit. The devices are mounted in an evacuated dewar held at 77 K and irradiated through a thin aluminum window with 2 MeV electrons from a Van de Graaf accelerator. Dose was calibrated by means of thermoluminescent detectors placed in the dewar. Dose rates were approximately 100 rad(ZnS)/sec (1 rad (ZnS) = .96 rad(Si) for 2 MeV electrons). All output circuitry except the floating gate is shielded from the electrons. All device irradiation and characterization is performed at 77 K. A typical device was irradiated in four or five incremental doses to a total dose of $10^5 \text{rad(ZnS)}$. Following each dose, the electron beam was turned off and the device was characterized. The entire process typically took 6 hours, during which time the device was constantly maintained at 77 K.

In the first set of experiments, the CCD gates were DC biased during irradiation to determine the dose dependence at constant bias of the radiation induced flatband shifts ($\Delta V_{FB}$) as determined from capacitance-voltage (C-V) measurements. In all DC bias experiments, the bias was on only for the short time that the irradiation was actually performed in order to avoid any long term bias induced flatband shifts [15]. The device received cumulative doses of .23, .6, 1.18, 1.54, and $3.32 \times 10^4 \text{rad(ZnS)}$ with the upper level gates biased at -10 volts and the lower level gates biased at -5 volts. Following each exposure, C-V measurements were made, and the flatband shifts were determined by comparison to pre-irradiation C-V data. These biases were chosen both to simulate CCD operating conditions and to allow investigation of flatband voltage shift as a function of insulator thickness at the same fields. In order to investigate annealing of the radiation induced flatband shifts, after the final dose the device was warmed to room temperature with all gates shorted to the substrate for 48 hours, and then recooled to 77 K for C-V characterization.

In the second set of experiments, the CCD gates on several devices on the same wafer were biased at different DC levels to determine the gate voltage dependence at a given dose of the radiation induced flatband shifts. In these experiments, the device received a dose of $2 \times 10^4 \text{rad(ZnS)}$. Following irradiation, C-V measurements were made to determine flatband shifts. The device was warmed to room temperature for 48 hours and then recooled to 77 K for further characterization as done previously.

In the final set of experiments, the CCD shift registers were operated continuously at a 100 kHz clock frequency during irradiation. Clock voltages for all gates are shown in Table 1. The device was completely cold shielded from 300 K background radiation to enable accurate determination of the dark current. In order to simulate the operation of the device as an imager, 50% of full well charge was injected continuously during irradiation using the tunnel input gate. Prior to irradiation, the performance of the device was fully characterized. Charge transfer efficiency was determined by measuring the loss in the leading edge of a series of equal input pulses. Dark current was determined by holding one phase of the CCD gates 'on' for many clock cycles while all of the other gates were off, integrating the charge generated under the 'on' gates, and then resuming normal clocking of the device to allow transfer of the integrated charge to the floating gate for output. Integrated dark current was measured as a function of both the integration time and the 'on' voltage for the gates under which charge was integrated. The maximum output voltage as a function of the lower level 'on' voltage was measured in order to determine effective well capacity as a function of this parameter. The actual voltage to charge conversion requires an estimate of the floating gate node capacitance (12 pF). The input-output transfer curve was determined by applying a 50 µsec pulse of varying magnitude to the input gate and measuring the resulting output voltage. The device was biased at -5, 1, and $1 \times 10^4 \text{rad(ZnS)}$. All clock voltages were maintained at pre-irradiation levels throughout the irradiation procedure. After each dose, dark current transfer efficiency, well capacity, and I-O transfer characteristics were measured. After $1 \times 10^4 \text{rad(ZnS)}$ C-V measurements were performed to determine the radiation induced flatband shifts produced during continuous operation. After the final dose, the device was warmed to room temperature for 48 hours with all gates shorted to the substrate, then recooled to 77 K for CCD performance evaluation and C-V characterization. A total

<table>
<thead>
<tr>
<th>Gate</th>
<th>Clock Voltages</th>
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<tbody>
<tr>
<td>$\phi_1$</td>
<td>'off' 'on'</td>
</tr>
<tr>
<td>$\phi_2$</td>
<td>-6.7 -12.0</td>
</tr>
<tr>
<td>$\phi_3$</td>
<td>-1.0 -5.1</td>
</tr>
<tr>
<td>$\phi_4$</td>
<td>0.0 -4.6</td>
</tr>
<tr>
<td>OG1</td>
<td>-5.0 -10.2</td>
</tr>
<tr>
<td>OG2</td>
<td>-6.7 -13.0</td>
</tr>
<tr>
<td>IG</td>
<td>0 -10.7</td>
</tr>
</tbody>
</table>

$V_{sub} = +4.1$
of 5 devices were irradiated using DC bias conditions and 3 devices were irradiated while operating as CCD shift registers. The specific results reported are typical of all devices characterized.

**EXPERIMENTAL RESULTS**

Flatband shift as a function of dose for the upper ($\phi_1$, $\phi_3$, OG1, OG2 in Figure 2) and lower ($\phi_2$, $\phi_4$, IG, FG in Figure 2) level gates is shown in Figure 3. Flatband shift was found to be linear with dose up to the maximum dose of $3 \times 10^4$ rad(ZnS). At that dose, a flatband shift of 4.5 volts was observed for first level gates biased at -5 volts, and a 8.5 volt shift was observed for the second level gates biased at -10 volts ($V_{sub}=0$). No change in the shape of the C-V curves was observed.

Flatband shift as a function of gate voltage for the upper and lower gate levels is shown in Figure 4 for a dose of $2 \times 10^4$ rad(ZnS). For both levels, a positive flatband shift was observed for irradiation under large negative bias, and a negative shift was observed for irradiation under positive bias. For the lower gate levels, a 1 volt shift is observed for a -6 volt bias and a -2 volt shift is observed for a 6 volt bias. Flatband voltages on devices that had been warmed to room temperature for 48 hours after irradiation and then recooled to 77 K were within 1 volt of their pre-irradiation values.

Prior to discussing the radiation effects on the operating characteristics of the CCDs, the pre-irradiation operating characteristics are discussed. Pre-irradiation charge transfer efficiency was 0.996 and full well capacity was $8 \times 10^{11}$/cm$^2$ (4x10$^6$ holes). The average carrier density resulting from a 1 msec integration of the dark current under the $\phi_2$ gates was $1.2 \times 10^{11}$/cm$^2$ (6x10$^5$ holes). If it is assumed that the carrier generation rate is constant, this corresponds to a dark current density of $1.9 \times 10^{-5}$ amps/cm$^2$. However, integrated dark current was highly nonlinear with time, and depended strongly on the 'on' voltage for the gate under which charge was collected during the integration period (Figure 5). Effective well capacity increased with decreasing (more negative) lower level gate 'on' voltage as would be expected. However, when the lower level gate 'on' voltage was decreased beyond approximately -5 volts, the effective well capacity (maximum output signal) decreased rapidly (Figure 6). This effect is not seen in CCDs fabricated in wider bandgap semiconductors. This effect and the gate voltage and time dependence of the integrated dark current are attributed to interband tunneling [16]. The pre-irradiation I-0 transfer curve is shown as the solid line in Figure 7, with the nonlinearity due to effects at the input and the output.

![Figure 3. Flatband shift ($\Delta V_{FB}$) vs. dose for DC biased lower ($\phi_2$) and upper ($\phi_1$) level (Hg,Cd)Te CCD gates.](image)

![Figure 4. Flatband shift ($\Delta V_{FB}$) vs. DC gate voltage for upper and lower level CCD gates on a single (Hg, Cd)Te wafer at a dose of $2 \times 10^4$ rad(ZnS).](image)

![Figure 5. Pre-irradiation integrated dark charge vs. $\phi_2$ gate 'on' voltage for a 1 msec integration.](image)
observed for doses less than $10^3$ rad(ZnS). At higher doses the dark current increased and the effective well capacity decreased. Consequently, after $10^4$ rad(ZnS) the dark signal charge collected in a 1 msec integration period saturated the CCD potential wells. The integrated dark current and effective well capacity as functions of total dose are shown in Figures 8 and 9, respectively.

![Figure 6. Pre-irradiation effective well capacity vs. $\phi_2$ gate 'on' voltage.](image1)

![Figure 7. Output voltage vs. input gate 'on' voltage pre-irradiation and after $10^4$ rad(ZnS).](image2)

The negative flatband voltage shift also biases the input gate so as to increase the fat zero level. After $10^4$ rad(ZnS) ($AV_{fb} = .5V$), the fat zero level has saturated the potential wells. With the input gate voltage reduced to eliminate signal saturation, a charge transfer efficiency of .992 was measured after $10^5$ rad(ZnS). The I-O transfer curve after this dose is compared to the pre-irradiation curve in Figure 7. C-V measurements at this point revealed a 2.2 volt flatband shift for the upper level gates, and a .5 volt flatband shift for the lower level gates. The shape of the C-V curves remained unchanged, however. After $10^5$ rad(ZnS) no output signal was observed with the device operating at pre-irradiation clock levels. By adjusting both the 'on' and 'off' clock voltages to compensate for the observed flatband shifts the pre-irradiation operating characteristics could be regained exactly. C-V measurements performed at 77 K on the device after it had been warmed to room temperature for 48 hours with all gates shorted to the substrate revealed that flatband voltages had returned to their pre-irradiated values. Clock voltages required for optimum CCD performance were nearly identical to those used prior to irradiation.

![Figure 8. Integrated dark charge vs. dose for a 1 msec integration time and pre-irradiation clock voltages.](image3)

![Figure 9. Effective well capacity vs. dose with pre-irradiation clock voltages.](image4)
The observed field and dose dependence of the flatband shifts for the CCD gates is consistent with that seen by Kalma et al. in their MIS capacitor studies [4]. Hole trapping under positive gate bias and electron trapping under negative gate bias at the (Hg,Cd)Te/ anodic oxide interface are the proposed mechanisms for the observed behavior. Several other studies have shown there to be a high density of traps at this interface also [17]. The linear dose dependence of the flatband shift indicates that saturation of the empty traps has not occurred at the maximum dose of 3x10^10 rad(Si). The increase of the upper level gate capacitance, and, hence, the insulator capacitance for the CCD gates, and the large stray capacitance of the gate interconnect lines, the accuracy with which the density of traps involved can be calculated is limited to ±20%. For the structure shown in Figure 1, assuming a dielectric constant of 18.5 for the anodic oxide and 7.5 for the ZnS, the flatband shift at the maximum dose for the first level gates corresponds to a net trapped charge density of 6.5x10^11/cm^2 if all the charge is assumed to be trapped at the interface. If we assume that the pair creation energy is 11 eV, then the net charge trapped is only approximately 3% of the total charge generated by the radiation. Making the same assumptions as above, one calculates a net trapped charge for the upper level gates of 8.7x10^11/cm^2. This behavior is consistent with the model of charge generation in the ZnS and transport to the (Hg,Cd)Te/anodic interface with trapping occurring at the interface. An additional 2.2x10^11 charges/cm^2 are trapped as a result of the additional ZnS thickness under the upper level gates. This corresponds to only .65% of the charge generated in the additional ZnS layer.

The gate voltage dependence of the radiation induced flatband shifts suggests that both electrons and holes are mobile in the ZnS. This is in contrast to SiO2 where only electrons are thought to be mobile at 77K [18]. The number of carriers which escape recombination or trapping contributes to a net trapped charge density which increases with the magnitude of the gate voltage. The data shown in Figure 4 imply a net trapping efficiency of .9% for the lower level gate areas when biased at -7 volts, corresponding to an insulator field of approximately 1.7x10^5 V/cm. For a 6 volt bias on the lower level gates, or an insulator field of approximately 1.5x10^6 V/cm, 95% trapping efficiency is observed. For the upper level gates, a trapping efficiency of approximately .7% is calculated for biases of 10 volts, corresponding to an insulator field of approximately 1.2x10^5 V/cm. The flatband shifts for the device used in obtaining the data in Figure 4 were approximately 1/3 of those seen in the device used to obtain the data in Figure 3 for the same bias and dose. Both devices were fabricated using the same process, but were processed at different times. This suggests that some uncontrolled processing parameter may strongly influence the properties of the ZnS and/or the anodic oxide which are associated with charge transport and trapping.

The results of the room temperature annealing experiments indicate that nearly all trapped charge is emitted from the traps upon warming. The fact that there is no change in the shape of the low temperature C-V curves after the annealing cycle suggests negligible interface state generation upon warming. In silicon MOS devices irradiated at 77K, interface state generation occurs only upon warming [19]. For hardened oxides, interface state densities on the order of 5x10^10/cm^2-eV are generated for a dose of 10^6 rad(Si). The changes in the operating characteristics of the (Hg,Cd)Te CCD which was operated continuously during irradiation were similar to those observed in silicon CCDs, but the mechanisms responsible for these changes are different in some cases. The decrease in effective well capacity with increasing dose can be associated with two effects. The unequal flatband shifts recorded after 10^4 rad(ZnS) result in a change in the potential profile in the (Hg,Cd)Te which leads to a decrease in the effective well capacity. This kind of effect has been observed in silicon CCDs [20]. For this device, calculations show that this effect reduces the usable well capacity by approximately 15% for the flatband shift with two effects. The unequal flatband shifts recorded in Figure 5, a positive flatband shift also results in a loss of usable well capacity due to tunneling current filling the wells. If the device is initially operated near maximum well capacity, this effect can be very dramatic, with a flatband shift of .5 volts resulting in a 45% decrease in effective well capacity on the steepest portion of the curve. When combined, these two effects account well for the approximately 55% decrease in effective well capacity which is observed after 10^4 rad(ZnS). The complete failure of the device after 10^5 rad(ZnS) is believed to be due to the increased tunneling caused by the positive radiation induced flatband shift. The possibility that the apparent loss in well capacity is due to a decrease in the gain of the floating gate and associated output circuitry because of flatband shifts is discounted because the clock voltages for the output section of the device alone did not affect the magnitude of the output signal. Readjustment of all the clock voltages in the direction suggested by the flatband shifts did, however, result in device operation at pre-irradiation well capacity even after 10^5 rad(ZnS).

The increase in dark current with increasing dose is also attributed to enhanced tunneling due to the positive radiation induced flatband shifts as suggested by Figure 5. Accurate qualitative agreement with flatband shift measured at 10^6 rad(ZnS) is not possible, but a .5 volt flatband shift from an initial operating voltage of -5.1 volts can be seen to result in approximately three-fold increase of the current after a pre-irradiation level of charge is collected during a 1 msec integration period, in good agreement with that observed experimentally after irradiation. Radiation induced flatband shifts for the field plate probably have some effect on the dark current because of edge field effects, but the radiation induced changes in this effect are expected to be small since the field plate flatband shifts are very small. It should be noted that for doses up to 10^6 rad(ZnS) the charge collected during a 1 msec integration could be reduced to pre-irradiation levels by increasing (making more positive) the 'on' voltage for the gate under which charge was being collected. This is taken as further evidence for tunneling being responsible for the increased dark current, rather than increased interface state or depletion layer generation.

The reason for degradation in transfer efficiency at these doses is not completely understood. Pre-irradiation transfer efficiency may be limited by a combination of effects including interface state trapping, bulk trapping, or interelectrode barriers. The temperature dependence of the transfer efficiency for these devices does not follow that expected from a simple model based on any one of the effects mentioned above alone. Even after a dose of 10^6 rad(ZnS) pre-irradiation charge transfer efficiency could be regained by adjusting the clock voltages, suggesting that radiation induced interface or bulk trapping effects are minimal. Also, no change in the shape of the C-V curves was observed after irradiation. C-V curve distortion
should be observable for the interface state density of approximately $2 \times 10^{11}$ cm$^{-2}$-eV which would be required to explain the observed decrease in transfer efficiency. It is important to note that the .992 transfer efficiency observed after $10^6$ rad(ZnS) would result in a severe degradation in MTF (<6) and hence image sharpness in an IR imager.

In considering techniques for improving the radiation hardness of CCD's, one considers both device design and operational mode changes to improve performance. The problems associated with tunneling are unique to interelectrode voltages in narrow bandgap semiconductors, and in this sense represent a new class of problems to be considered in the radiation hardening of devices. Three approaches are required to minimize this effect: hardened insulators which result in smaller flatband shifts for a given dose, improved quality semiconductor material which is less susceptible to impurity or defect related tunneling, and device design which minimizes high field regions where tunneling effects are strongest. With regard to improving insulator hardness, Kalma et al. have shown that photochemically deposited SiO$_2$ is less susceptible to radiation induced flatband shifts than thermally grown SiO$_2$ [21]. Koch et al. have also fabricated (Hg,Cd)Te CCDs using this Insulator [22]. It is expected that these devices would show enhanced radiation hardness. With regard to semiconductor material improvement, there is evidence that p-type (Hg,Cd)Te is less susceptible to defect level related tunneling than n-type (Hg,Cd)Te [23], so that an n-channel device might be harder in this respect. It should be noted, however, that because of the observed gate voltage dependence of the flatband shift for the ZnS/anodic oxide based devices, that an n-channel device using this insulator irradiated during operation would still suffer from radiation induced flatband shifts in the direction leading to enhanced tunneling. The reduction in effective well capacity due to unequal flatband shifts for different gate levels is a problem inherent in the dual layer insulator design and can be avoided by using p-channel n-type insulator with some technique for controlling interelectrode potentials. The radiation hardness of the input section of the device could be enhanced by including an input structure capable of operation in the 'potential equilibration' mode. This input would allow post irradiation operation with post irradiation operation with 2-3 volt flatband shifts [24].

With regard to improving hardness by operational mode changes, for the device studied in this work, it can be seen that if one were willing to sacrifice pre-irradiation well capacity and operate at less negative lower level gate voltages initially, then one could shift the onset of tunneling associated device failure to higher doses.

**SUMMARY**

Flatband shifts as functions of both dose and DC gate bias were measured for (Hg,Cd)Te CCD gates irradiated with 2 MeV electrons at 77 K. Positive flatband shifts associated with hole trapping at the semiconductor/insulator interface were observed for irradiation under negative bias. Negative flatband shifts associated with electron trapping at the semiconductor/insulator interface were observed for irradiation under positive gate bias. The trap density associated with both effects was greater than $6 \times 10^{11}$ cm$^{-2}$. Typical flatband voltage shifts for thick insulator areas of the device were 3 volts for a dose of $1 \times 10^6$ rad (ZnS).

A (Hg,Cd)Te CCD was operated continuously during irradiation in a 2 MeV electron beam. Effective well capacity decreased and integrated dark current increased with increasing dose. At $10^4$ rad(ZnS) effective well capacity had been reduced by 50% to $4 \times 10^{12}$ cm$^{-2}$, and dark current had increased by a factor of three from its pre-irradiation value. A full well result was observed from a 1 MeV irradiation of the dark current. Charge transfer efficiency had degraded to .992, a value which would result in serious degradation in image quality in an IR imager. After $10^3$ rad(ZnS) the device no longer operated with pre-irradiation clock levels. At this dose the device would completely fail as an imager if the clock voltages could not be adjusted due to changes in operation as a result of trapping.

The radiation sensitivity of these (Hg,Cd)Te CCDs at 77 K appears to be comparable to that observed for the thermal oxide silicon CCD's which are used in the hybrid focal plane infrared imagers.

**ACKNOWLEDGEMENTS**

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