This paper describes the effects of ionizing radiation on charge-coupled-devices (CCDs) at 80°K. The CCDs were fabricated with an oxide/nitride (MNOS) dual dielectric gate insulator used for its excellent radiation tolerance at cryogenic temperatures. A novel hydrogen implantation process was employed to obtain improved CCD electrical performance through an extremely low density of interface states at the oxide-silicon interface.

N-surface-channel and N-buried-channel MNOS CCDs have been fabricated and irradiated at 80°K. Both CCD types operate following 10⁶ Rad(Si) exposure. Radiation-induced degradation in CCD charge transfer efficiency is much worse in the surface-channel CCD compared to the buried-channel CCD. A model involving formation of potential energy wells due to charge trapping in the insulators between polysilicon gates is proposed to explain this effect. Measurements of the interface state density in the CCDs and test capacitors show that generation of interface states by ionizing radiation is almost completely suppressed at 80°K.

INTRODUCTION

The effect of ionizing radiation on silicon MOS devices has been shown to be substantially enhanced at cryogenic temperatures (<100°K) compared to 295°K due to increased trapping of radiation-generated holes in the oxide which results in large threshold voltage shifts[1,2]. In addition, this effect appears to be independent of oxidation type or process [2]. For example, it has been demonstrated that a CCD fabricated with a radiation-hard "process-optimized" oxide with a threshold voltage shift of -2.2V at 10⁶ Rad(Si) at 295°K has the same shift when cooled to 90°K at only 1.4x10⁴ Rad(Si)[3]. However, there are space-based and military applications for CCD infrared focal plane imagers and signal processors which operate at cryogenic temperatures (10-100°K) and which will be required to operate in ionizing radiation environments.

To address this requirement for a radiation-hard insulator for cryogenic applications, alternative approaches such as ion-implanted oxides, device operation at high electric fields, very thin gate oxides, and dual dielectric insulators (such as MNOS) have been proposed[4,5]. Of these approaches, only the use of a dual dielectric MNOS (metal-nitride-oxide-semiconductor) has been successfully demonstrated to date in a radiation hard CCD test structure[5,6]. Flatband voltage shifts as small as -1.0V/10⁶ Rad have been measured at 80°K on MNOS test devices with appropriate thicknesses of the nitride and oxide layers[7]. In the MNOS insulator, a thin thermally grown oxide provides a high quality silicon oxide interface necessary for proper CCD operation. Optimum radiation tolerance is achieved with the thinnest possible oxide which, however, must be thick enough to prevent tunneling of carriers from the silicon to the oxide nitride interface. Typical thicknesses of the MNOS layers are approximately 10 nm oxide/50-100 nm nitride.

In the past, a major drawback to the use of the MNOS structure has been a relatively high density of interface states Dᵢₛ. Using conventional high temperature annealing, the lowest achievable Dᵢₛ was approximately 2x10¹⁰/cm²-eV, a value too high to fabricate surface-channel CCDs with acceptable charge transfer efficiency [5,6]. A new technique, hydrogen implantation, has been developed to fabricate MNOS SC-CCDs with much reduced Dᵢₛ (typically about 1x10⁷/cm²-eV at mid-gap) and much improved transfer efficiency [8,9].

If possible, it would be desirable to develop radiation-hardened versions of both a surface-channel (SC) and buried channel (BC) MNOS CCD. Each type has its own relative advantages and disadvantages—for example, the SC-CCD has a higher signal charge capacity (useful in hybrid IR focal plane array technology), while the BC-CCD has a much better transfer efficiency. Considering radiation-hardening, there are two significant differences between SC and BC devices: (1) Threshold voltage shifts in the MNOS insulators depend on the electric field in the insulators during irradiation [7] (see fig. 3), and the electric field is a function of the device type. For typical operating conditions, the (N-channel) SC-CCD should be more radiation tolerant than the (N-channel) BC-CCD [5]. (2) The SC-CCD is much more sensitive to the creation of interface states by ionizing radiation because the signal charge in the SC-CCD is in intimate contact with the interface, whereas signal charge in the BC-CCD resides several hundred nanometers away from the interface. However, recent measurements have shown that the formation of interface states by ionizing radiation is either substantially reduced or completely suppressed when cooled to 80°K [6,10,11]. Thus it is desirable to determine whether there is sufficient suppression of interface state formation by radiation at 80°K to achieve a radiation-hard SC-CCD. Recent work on p-channel SC-CCDs has demonstrated substantial, but not complete, suppression [6].

In this work, the radiation tolerance of CCDs fabricated with the hydrogen implantation techniques is determined. Radiation effects are reported for MNOS test structures and CCDs with extremely low interface state density (Dᵢₛ<1x10⁷ states/cm²-eV). Both N-surface- and N-buried-channel CCDs are operational following 1x10⁶ Rad(Si) dose at 80°K. These are the first reported radiation effects on N-channel CCDs fabricated with radiation-hard MNOS CCD technology; previous measurements have been on p-channel devices [5,6]. No significant degradation in the radiation tolerance of the MNOS structure due to the hydrogen implant process is observed.

CCD FABRICATION

The fabrication process for the N-channel CCDs is shown in Table I. For clarity, only the high temperature and photoengraving steps are shown. This is a typical N-channel CCD process which includes phosphorus gettering for high minority carrier lifetime, field region self-aligned to the P⁺ channel stop, two levels of phosphorous doped polysilicon gates, and an aluminum interconnect level. The MNOS gate insulators are formed by a 10 nm (nominal) oxidation in O₂ at 900°C and 50-100 nm silicon nitride deposited by chemical vapor deposition (deposition of SiCl₂H₂ at 800°C and atmospheric pressure). A very thin (<5 nm) oxide layer is grown on top of the gate nitride using a pyrogenic oxidation (step 14, Table I); this step has been found necessary to obtain MNOS structures with good structures with good stability following accelerated aging (temperature bias stress) testing [12].

ABSTRACT


Radiation Effects in N-Channel MNOS CCDs at Low Temperature

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20375

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TABLE I

<table>
<thead>
<tr>
<th>STEP</th>
<th>PURPOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PYROGENIC OXIDATION, 1000 nm</td>
</tr>
<tr>
<td>2</td>
<td>PHOTORESIST FORMATION</td>
</tr>
<tr>
<td>3</td>
<td>PHOSPHOROUS DIFFUSION, 1900°C</td>
</tr>
<tr>
<td>4</td>
<td>PYROGENIC OXIDATION, 80 nm</td>
</tr>
<tr>
<td>5</td>
<td>DEPOSITION 80 nm SILICON NITRIDE</td>
</tr>
<tr>
<td>6</td>
<td>PHOTORESIST FORMATION</td>
</tr>
<tr>
<td>7</td>
<td>BORON IMPLANT</td>
</tr>
<tr>
<td>8</td>
<td>PYROGENIC OXIDATION, 200 mm, 100°C</td>
</tr>
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<td>9</td>
<td>PHOTORESIST FORMATION</td>
</tr>
<tr>
<td>10</td>
<td>PHOSPHOROUS IMPLANT</td>
</tr>
<tr>
<td>11</td>
<td>ETCH OXIDES, NITRIDE FROM GATE REGION</td>
</tr>
<tr>
<td>12</td>
<td>PYROGENIC OXIDATION, 10 nm</td>
</tr>
<tr>
<td>13</td>
<td>DEPOSIT 80 nm SILICON NITRIDE</td>
</tr>
<tr>
<td>14</td>
<td>PYROGENIC OXIDATION @ 100°C</td>
</tr>
<tr>
<td>15</td>
<td>500 nm POLYSILICON DEPOSITION</td>
</tr>
<tr>
<td>16</td>
<td>PHOSPHOROUS DIFFUSION, 1000°C, 1000°C, 80°C</td>
</tr>
<tr>
<td>17</td>
<td>PHOTORESIST FORMATION</td>
</tr>
<tr>
<td>18</td>
<td>PHOSPHOROUS OXIDATION @ 1200°C</td>
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<tr>
<td>19</td>
<td>500 nm POLYSILICON DEPOSITION</td>
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<td>20</td>
<td>PHOSPHOROUS DIFFUSION, 900°C</td>
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<td>PHOTORESIST FORMATION</td>
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<td>22</td>
<td>PHOTORESIST FORMATION-CONTACT VIAS</td>
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<tr>
<td>23</td>
<td>1000 nm ALUMINUM DEPOSITION</td>
</tr>
<tr>
<td>24</td>
<td>PHOTORESIST FORMATION</td>
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<tr>
<td>25</td>
<td>HYDROGEN IMPLANT</td>
</tr>
<tr>
<td>26</td>
<td>450°C ANNEAL</td>
</tr>
</tbody>
</table>

The hydrogen implantation process used to achieve an extremely low density of interface states in these devices has been described in some detail previously [7,8] and will be described only briefly here. A cross section of the MNOS insulators in the gate and insulator field regions of the CCD is shown in Fig. 1. The nitride layer is continuous across the gate and field regions. The CCD is implanted at 0.5-3x10^16 H^+ cm^-2 after all other processing, including polysilicon gates and aluminum interconnect lines, is complete. The implant energy of 7-8 kV is chosen to place the peak of the implanted hydrogen profile in the field oxide just beneath the nitride layer. At this energy the range of the hydrogen ions is too short to penetrate the thick polysilicon gate and only the field region is implanted; thus the sensitive MNOS gate insulators are protected from damage caused by the relatively high fluence implant. A 450°C two hour anneal is then used to drive the implanted hydrogen laterally from the field oxide into the thin gate oxide where it acts to reduce the interface state density. The nitride layer and the single crystal silicon have very low rates of hydrogen diffusivity compared to silicon dioxide, and therefore the silicon and the nitride serve to contain the hydrogen in the oxide layers during the anneal.

A relatively simple CCD structure was chosen for the initial implementation and testing of the hydrogen implantation technique. Changes in design (for example, to an area array) or fabrication technology (such as a thicker field oxide or phosphorous reflow glass for step coverage) will require additional research on ways to implement the hydrogen implant process.

EXPERIMENTAL DETAILS

IRRADIATION

Devices were irradiated at the NRL Co^60 source at a dose rate of approximately 8x10^5 Rad(Si)/min. The devices are bonded in 28-pin ceramic dual-in-line packages and securely clamped to an aluminum cold finger connected to a liquid nitrogen reservoir inside a vacuum dewar. Using this dewar, the CCD may be operated while cooled at the end of a 20 ft cable at the bottom of the Goat pool. Each device was irradiated in incremental doses to a total dose of 10^6 Rad(Si) and characterized following each incremental dose. The entire process typically took about 32 hours, during which time the device was continuously maintained at 80°C.

CCD OPERATION AND MEASUREMENT TECHNIQUES

The CCDs are 4-phase linear shift registers with electrical input and reset amplifier output as shown in the CCD cross section of Fig. 2. The structure of the BC- and SC-CCDs is exactly the same except for the buried-channel itself; note that in the BC-CCD, the N+ diffusion is buried-channel but the output amplifier lacks the buried-channel. This affects the threshold voltage shift at the output (see discussion below).

Fig. 1. CCD cross section showing structure of the MNOS insulators in the gate and field insulator regions. Excellent radiation hardness is obtained due to the very thin oxide layer. The continuous nitride layer in the field region is required for the hydrogen implantation technique.

Fig. 2. CCD cross section showing CCD structure at the electrical input, transfer section, and output amplifier. The amplifier consists of a dual-gate reset transistor and output transistor operated as a source-follower (the output transistor is on-chip but shown separately for clarity).

Most of the testing was accomplished using either 140- or 20-bit CCDs with a bit size of 30μm by 100μm, although a few measurements were also made on 105- or

- Diagram of MNOS CCD fabrication process (Abbreviated)
- Table listing steps and purposes of each step in the fabrication process
- Description of the hydrogen implantation process and its effects on device performance
- Experimental details for irradiation of devices
- Diagram of CCD structure and operation
15-bit CCDs at 40μm by 100μm. Other devices including transistors and capacitors are also available on each chip for test purposes, and a few measurements of transistor characteristics in the low-field regime obtained on large area transistors (500μm by 500μm) are described later (Fig. 4).

The CCDs were operated as dynamic shift registers at 250 kHz with phase clock swings of +2 to +10V (SC-CCD) or -7 to +8V (BC-CCD) (referred to the substrate). During operation, the electric fields in the oxide of the MNOS insulator (CCD transfer section) are typically 1-2x10^5 V/cm in the SC-CCDs and ~5x10^5 V/cm in the BC-CCDs (calculated for no signal charge under the MNOS gate, a condition which exists for a minimum of 95% of the time during operation). Note that the electric field in the BC-CCD is reversed and increased in absolute magnitude compared to the SC-CCD, which will have a strong effect on the threshold voltage shift (see Fig. 3).

Threshold voltage shifts at the CCD input gate were obtained by measuring the input gate voltage required to obtain a small (100 mV) signal at the CCD output with fixed dc bias on the input diode. Threshold voltage shifts in the source-follower output transistor were obtained by measuring the output voltage at the source of the transistor and multiplying by a small correction factor to account for the voltage gain of the source follower which is typically about 0.9 for a 10 kohm load resistor. The source follower transistor gate is 8μm long by 12μm wide with the same MNOS gate insulator as the rest of the CCD. In order to convert a voltage measured at the output of the CC to signal charge, the charge amplification of the CCD output amplifier, typically about 9x10^13 coul/V, was measured for each device after each incremental irradiation. The gain of this amplifier decreased by less than 5% for all devices measured up to 10^6 Rad(Si).

The density of interface states in the CCDs was measured by the periodic pulse technique [16,17]. A group (or "burst") of about 5 charge packets is entered into the CCD which is operated continuously as a shift register. The burst is transferred to the output where the loss in the first packet Qloss is measured. Qloss is given by [16]:

\[ Q_{\text{loss}} = q \times TA \times D_{\text{it}} \times \ln(t_b/T) + C \]

where the first term describes the loss due to interface states and is a function of the time between bursts \( t_b \), \( C \) is a constant loss due to all other sources besides interface states and assumed to be independent of \( t_b \), \( A \) is the total CCD area, and \( T \) is the CCD transfer time (\( T = 1 \) μs for 250 kHz operation with 4-phase clocks). Because \( C \) is unknown, \( D_{\text{it}} \) is obtained by measuring \( Q_{\text{loss}} \) as a function of \( t_b \) which is varied from 10^-5 to 1 second and calculating \( D_{\text{it}} \) from the slope of \( Q_{\text{loss}} \) plotted versus \( \ln(t_b) \) (for an example, see Fig. 5 in ref. [17]). Note that the periodic pulse technique is applicable to BC-CCDs as well as SC-CCDs so long as the signal charge packets are large enough to exceed the capacity of the buried-channel and interact with the interface states [17]. It is estimated that using the periodic pulse technique, values of \( D_{\text{it}} \) are accurate to ±15, ±40%, where the major source of error is edge effects which prevent the charge packets from contacting the interface states near the edges of the gates which results in an overestimation of the effective area \( A \) [17]. Relative values of \( D_{\text{it}} \) between devices of the same geometry, or the same device at different doses, do not suffer from this effect and are more accurate, estimated at ±15%. Although Eq. (1) is derived with the assumption that there is no energy dependence of \( D_{\text{it}} \) (\( E \)), in practice this restriction may be relaxed as long as \( D_{\text{it}} \) is "slowly varying," a condition satisfied by the devices here.

EXPERIMENTAL RESULTS

PRE-IRRADIATION CCD CHARACTERISTICS

A summary of CCD devices and pre-irradiation characteristics is shown in Table II. The devices were obtained from three wafers (two SC and one BC) from two different process lots. MNOS insulator thicknesses were measured on test pieces and may vary by ±10% on the actual CCDs. The 100 nm thickness of the nitride layer in lot 4-7 is considerably thicker than the design goal of 70 nm due to an error in processing.

<p>| TABLE II |
|-----------------|-----------------|-----------------|-----------------|-----------------|</p>
<table>
<thead>
<tr>
<th>CCD PROCESS</th>
<th>LOT</th>
<th>WAFER #</th>
<th>DEVICE TYPE</th>
<th>MNOS OXIDE THICKNESS (nm)</th>
<th>NITRITE THICKNESS (nm)</th>
<th>MIDGAP D_\text{it} \times 10^3 \mu A/V/CM²</th>
<th>TRANSFER EFFICIENCY</th>
<th>295°K</th>
<th>30°K</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4</td>
<td>2</td>
<td>SC</td>
<td>9.4</td>
<td>75</td>
<td>1.6 x 10^4</td>
<td>5 x 10^-5</td>
<td>2.5 x 10^-4</td>
<td>4.7</td>
<td>4</td>
</tr>
</tbody>
</table>

Using the hydrogen implantation technique, CCDs have been fabricated with typical midgap \( D_{\text{it}} \) of 8x10^8/cm²-eV (BC-CCDs) and 1.5x10^9/cm²-eV (SC-CCDs) as measured by the CCD periodic pulse technique at room temperature. When cooled to 80K, measured values of \( D_{\text{it}} \) are typically somewhat higher (Table II); this apparent increase occurs because \( D_{\text{it}} \) is measured much closer to the conduction band edge at the lower temperature where \( D_{\text{it}} \) is typically observed to be greater than its midgap value [13]. These results are in reasonable agreement with measurements of midgap \( D_{\text{it}} \) obtained by a simplified ac conductance technique [14] on on-chip test capacitors in the range 0.5-2.0x10^9/cm²-eV. These \( D_{\text{it}} \) values are approximately an order of magnitude smaller than reported previously for p-channel MNOS CCDs [5,6].

Measurements of transfer inefficiency \( \epsilon \) (\( \equiv \) 1-efficiency) shown in Table II are all made without bias charge (or "fat zero") which is a technique to constantly maintain a small signal in the CCD to reduce charge trapping and thereby improve the transfer efficiency. Pre-irradiation \( \epsilon \) in the SC-CCDs is very good, typically 1x10^-4 or less at 295K, which reflects the very low values of \( D_{\text{it}} \) in these devices. Substantial improvement in \( \epsilon \) is observed in the SC-CCDs with the addition of bias charge; for example, a factor of 2-3 improvement is obtained with 5% (of the maximum signal) bias charge. \( \epsilon \) is somewhat higher for both CCDs at 80K compared to 295K because of increased \( D_{\text{it}} \) near the conduction band edge in the SC-CCDs and the onset of electron trapping by donors on the buried-channel in the BC-CCD [15]; both effects have been observed previously and are not related to the MNOS gate insulator structure.

RADIATION EFFECTS IN TEST STRUCTURES

In order to model the threshold voltage shifts in the complex CCDs, MNOS test capacitors with 9.0 nm oxide/77 nm nitride were fabricated and radiation tested at 80K. Flatband voltage shifts \( AV_{\text{fb}} \) obtained from MxR C-V data have been measured as a function of gate bias applied during irradiation as shown in Fig. 3 for a total dose of 10^6 Rad(Si). The absolute magnitude of \( AV_{\text{fb}} \) is quite small, in the range -1 to -2V,
due to the thinness of the oxide layer and some electron trapping in the nitride layer which compensates the trapped holes in the oxide. The CCDs operate with electric fields at the interface which are usually much less than 1.0x10^6 V/cm, which corresponds to the gate bias range between -5 and +5V in Fig. 3. \( \Delta V_{fb} \) is larger at negative gate bias compared to positive gate bias as observed previously [7]; however, the shift at moderately negative gate bias is somewhat smaller in this work due to the combined effects of thinner insulator layers and the high temperature oxidation step that the nitride is now exposed to (step 14, Table I).

In Fig. 3, data is shown from three samples from a single wafer of test capacitors which differ only by the amount of implanted hydrogen used to reduce the interface gate density. Two samples are implanted with 5x10^16 H+/cm² and 1x10^16 H+/cm², and the third sample is an unimplanted control. There are only minor differences in the \( \Delta V_{fb} \) data for these samples, differences which are less than the sample-to-sample variations typically observed and which are mainly caused by variations in nitride thickness across the wafer. Therefore, the data in Fig. 3 demonstrates that the hydrogen implant process does not degrade the MNOS radiation hardness.

A limited amount of flatband voltage shift data has been obtained on on-chip capacitors from a CCD wafer (process lot 4-7, wafer 2). This data shows a similar dependence of \( \Delta V_{fb} \) on gate bias during irradiation as in Fig. 3; however, the measured shifts were 20-40% larger, apparently due to the slightly thicker gate nitride layer.

In order to insure that the measured flatband voltage shifts are representative of threshold voltage shifts in actual transistors and CCDs, a few measurements were made on MNOS test transistors from process lot 4-4, wafer 2. Transistor drain current was measured in the low-field linear regime with a 50 mV source-to-drain voltage for large area 500µm x 500µm transistors irradiated at 80°K with the gate tied to the substrate as shown in Fig. 4 for total doses of 0, 1x10^6, and 2x10^6 Rad(Si). The main effect of the radiation may be described as a parallel shift of the transistor characteristic to more negative gate voltage. The threshold voltage shift from this data is -0.60V at 1x10^6 Rad(Si) and -0.96V at 2x10^6 Rad(Si) measured at 1mA drain current, somewhat smaller than the data from test capacitors shown in Fig. 3.

A second order effect shown in Fig. 4 is that the subthreshold transistor characteristic is not quite as steep a function of \( V_g \) following irradiation, an effect which is probably caused by increased lateral non-uniformities of the trapped charge in the irradiated devices. The low-field inversion layer electron mobility in these transistors is high (3.0x10^5 cm²/V-s) at 80°K, an indication of the high quality interface obtained in the MNOS structure. No decrease in electron mobility was observed following 2x10^6 Rad(Si) dose. At 295°K the peak mobility is about 900 cm²/V-s.

In addition to measuring flatband voltage shifts, the density of radiation-induced interface states has been measured in MNOS test capacitors by a simplified but very sensitive ac conductance technique [14]. \( D_{it} \) for capacitors irradiated at 295°K and 80°K with +5V applied to the gate during irradiation is shown in Fig. 5. At 295°K, \( D_{it} \) increases from a pre-irradiation value of 3x10^10 states/cm²-eV to 1.1x10^12/cm²-eV at 10^6 Rad(Si). However, at 80°K, essentially no increase in \( D_{it} \) is observed from the pre-irradiation value of about 1x10^9/cm²-eV. This data in Fig. 5 demonstrates the effectiveness of reduced temperature in suppressing the formation of interface states. This data is in qualitative agreement with previous reports of suppression of interface state generation at low temperatures in MOS capacitors [10,11] and p-channel MNOS CCDs [6]. It is estimated that the error in \( D_{it} \) for the data in Fig. 5 is ±0.460% for the 295°K data but is much less accurate, ±0.4300%, at 80°K due to the strong effect of lateral non-uniformities due to fixed charge on the ac conductance data. To some extent the increase in \( D_{it} \) at 80°K was a function of gate bias during irradiation, particularly at negative gate bias, and large increases in \( D_{it} \) were observed for gate biases < -5V during irradiation.

**CCD THRESHOLD VOLTAGE SHIFT**

Threshold voltage shifts \( \Delta V_{fb} \) have been measured in N-SC and N-BC MNOS CCDs irradiated while operating continuously as shift registers at 80°K. \( \Delta V_{fb} \) at the input gate and output transistor for a typical SC-CCD
and BC-CCD from process lot 4-7 are shown in Figs. 6 and 7, respectively.

Fig. 6. Threshold voltage shifts $\Delta V_{th}$ vs total dose for SC-CCD. Shift is larger at the input gate compared to the output transistor due to different effective electric fields during irradiation. Results are in good agreement with test capacitor data (Fig. 3).

At the SC-CCD output transistor, $\Delta V_{th} = -1.1$V is measured at $10^6$ Rad(Si) total dose (Fig. 6). This is in reasonable agreement with the flatband voltage shifts observed for MNOS test capacitors biased at $V_g = 0$ to $+5$V, which is the effective gate bias range of the output transistor during operation. This transistor is operated in the large signal mode with a large source-to-drain voltage drop (approx. 7V) such that the electric field in the gate insulator varies as a function of position along the transistor channel length, and therefore exact correlation with test capacitor measurements is not expected.

Fig. 7. Threshold voltage shifts $\Delta V_{th}$ vs total dose for BC-CCD. The shifts at both the input gate and output transistor are about a factor of two larger than anticipated from results on test capacitors (Fig. 3) and the SC-CCD (Fig. 6), perhaps caused by processing errors during deposition of the gate nitride.

At the SC-CCD input gate, $\Delta V_{th} = -2.1$V is measured at $10^6$ Rad(Si) total dose (Fig. 6). This value is almost twice that measured at the output transistor, although the MNOS insulators in the two structures should be the same; the different shifts are caused mainly by the different effective gate bias conditions while operating during irradiation. The bias applied to the input gate is a $-5$ to $+8$V pulse with most of the time (>$90\%$) spent at $-5$V. These results are at least qualitatively consistent with the threshold voltage shifts obtained on test capacitors (Fig. 3) which show larger shifts at negative gate voltages.

$\Delta V_{th}$ for the BC-CCD irradiated while operating at 80K is shown in Fig. 7. $\Delta V_{th}$ is about a factor of 2 larger at the CCD input gate compared to the output transistor, similar to the SC-CCD data. The input and transfer sections of the BC-CCD operate at negative electric field in the MNOS insulators due to the effect of the (depleted) buried-channel, and therefore from the data on test capacitors (Fig. 3) these sections are expected to show larger shifts than the SC-CCD. However, the output transistor of the BC-CCD is identical to the SC-CCD (i.e., no buried-channel in the BC-CCD output stage) and also is biased in exactly the same manner, so the same shift should have been observed. This difference is not understood; however, the larger $\Delta V_{th}$ in the BC-CCD may be due in part to a more radiation sensitive MNOS structure, perhaps related to the processing error which produced nitride layers in lot 4-7 considerably thicker than desired (Table II).

With the particular CCD devices available, it was not possible to measure $\Delta V_{th}$ directly on the CCD transfer gates. However, because these gates typically operate at relatively low electric field most of the time (see "CCD Operation") where $\Delta V_{th}$ is at a minimum, shifts in the CCD transfer gates are expected to be at least no worse than the data shown in Figs. 6 and 7. The threshold voltage shift data in these two figures although complicated by the effects of gate bias, show that the shifts observed in the operating devices are not substantially worse than expected from the test capacitor results (especially when thicker nitride in the CCDs is accounted for), and that the devices are reasonably radiation hard.
Measurements of CCD transfer inefficiency for an SC-CCD and BC-CCD irradiated while operating at 80°K are compared in Fig. 8 as a function of total dose up to 1x10^6 Rad(Si). This data was obtained on the same devices used for the data in Figs. 6 and 7, and it is representative of the total of 10 devices irradiated at 80°K in this work.

The most important feature of the CCD transfer efficiency data in Fig. 8 is that both devices survive 10^6 Rad and continue to operate without change in the operating biases. A moderate increase in transfer efficiency is observed in the BC-CCD at exposures above 1x10^5 Rad. This effect is most likely caused by effective changes in the operating points due to threshold voltage shifts which may be as large as -4V at 10^6 Rad (see Fig. 7). It is also possible that part of the degradation is related to the formation of potential barriers in the interelectrode regions (see Fig. 11 and related discussion). For actual applications, it is anticipated that the maximum allowed threshold voltage shift in the CCD transfer section would be no more than -1V; thus the BC-CCD should be considered "radiation-hard" to about 2x10^5 Rad. With a reduction in the thickness of the nitride to about 50 nm, the radiation tolerance should be improved by nearly a factor of 2.

As shown in Fig. 8, transfer inefficiency $\varepsilon$ in the SC-CCD increases dramatically with dose from 1.7x10^{-4} pre-irradiation to 5.5x10^{-2} at 10^6 Rad. Although substantial improvement in SC-CCD transfer efficiency may be obtained by operating with a small amount of bias charge (Fig. 9), the basic trend of increasing $\varepsilon$ with increasing dose remains the same. To confirm this experimental observation, three SC-CCDs from a different process lot (lots 4-7) were irradiated at 80°K with 0, +5 or -5V on all gates during irradiation. All three devices showed an increase $\varepsilon$ commensurate with the data in Fig. 8. Thus this effect has been reproduced for several devices from each of two completely independent process lots and has also been shown not to depend on the gate bias during irradiation.

This large increase in $\varepsilon$ in SC-CCDs irradiated at 80°K was not anticipated before the experiment was performed. In an SC-CCD, the transfer efficiency at frequencies below about 10 MHz is usually controlled by interface state trapping. Since previous measurements and results on MNOS capacitors in this work (see Fig. 5) show that interface state generation by ionizing radiation is suppressed at 80°K, no change in SC-CCD transfer efficiency would be expected.

It is possible that, despite previous results, interface states may be created in the SC-CCD by radiation at 80°K due to some unknown, unique feature in the CCD processing or structure. In order to check this hypothesis, interface state densities in several MNOS BC-CCDs from process lot 4-7 have been measured by the periodic pulse technique following irradiation at 80°K. As shown in Fig. 10, only a very slight increase in $D_{it}$ of 1.7x10^9 states/cm^2-eV at 10^6 Rad is observed in the BC-CCDs. This increase is not nearly large enough to explain the degradation in SC-CCD transfer efficiency.

Another possible cause of the degradation is the formation of potential energy barriers or wells due to trapping of radiation-induced charge in the insulators between the polysilicon gates. A cross-section of this region is shown in Fig. 11 (top). A considerable amount of charge will be created by radiation in the relatively thick (250 nm) oxide between the polysilicon layers. The holes will be trapped throughout that oxide, while trapping of the relatively mobile electrons will probably occur at the nitride/inter-gate oxide interface just as it has been shown to occur at the gate oxide/nitride interface of the gate MNOS insulators [18]. While a detailed analysis of this effect must await detailed two-dimensional mathematical modeling, it is clear that significant net charge trapping of either polarity may cause the formation of a potential barrier or well in the interelectrode region which reduces CCD transfer efficiency [19,20]. At 80°K
Potential and trapped charge suppression in oxide/nitride interfaces, shown in Fig. 11, was achieved at relatively even temperatures (80°K) by ionizing radiation at room temperature. This suppression was almost completely maintained at liquid nitrogen temperature. The question arises, at what temperature does interface state formation begin? An approximate answer may be obtained by irradiating a CCD at 80°K and measuring D_trapped charge efficiency as shown at the bottom of Fig. 11. A similar effect was observed previously.

Assuming that trapping of positive charge in the interelectrode oxide dominates electron trapping at the oxide/nitride interface, the net positive charge will cause a spurious potential well to form between adjacent phase gates in an N-channel CCD. This will cause reduced transfer efficiency as shown at the bottom of Fig. 11. A similar effect was observed previously.

In the BC-CCD, charge transfer occurs close to the metallurgical junction of the buried-channel and substrate, far (approx. 500 nm) from the insulators. At this distance, the fringe electric field from the gates is much more effective at negating any small potential well or barrier caused by charge trapped in the interelectrode region [20]. Thus, the proposed model explains why the transfer efficiency degradation is much worse in the SC-CCD compared to the BC-CCD.

**CCD Annealing**

It has been shown in this work and elsewhere [6,10,11] that the formation of interface states usually observed in MDS devices following exposure to ionizing radiation at room temperature is almost completely suppressed at liquid nitrogen temperature. The question arises, at what temperature does interface state formation begin? An approximate answer may be obtained by irradiating a CCD at 80°K and measuring D_trapped charge efficiency as shown at the bottom of Fig. 11. A similar effect was observed previously.

In Fig. 12, D_trapped charge for a BC-CCD irradiated to 5x10^5 Rad Si at 80°K is shown as a function of the annealing temperature. The CCD was operated continuously as a shift register during the anneal time (360 min to 280°C). A small decrease in D_trapped charge is measured at the start of the anneal (80°K-90°C); the cause of this is not known but is believed to be a measurement artifact. An increase in D_trapped charge is observed for temperatures above 110°K. Once warmed to room temperature, the formation of interface states is essentially complete; an additional 16 hours at 295°C caused only a 20% increase in D_trapped charge measured on a different device. The increase in D_trapped charge is clearly permanent since D_trapped charge does not decrease to its initial value upon re-cooling. This data suggests that temperatures below 100°C are required for complete suppression of interface state formation.

**Summary**

N-channel MNOS CCDs and associated test devices have been fabricated, irradiated, and characterized at 80°C. A new fabrication process, hydrogen implantation, has been utilized to obtain devices with an extremely low density of interface states (midgap D_trapped charge ~ 1x10^12 states/cm^2 eV). Measurements of flatband voltage shift in irradiated MNOS capacitors show that the
model 4204 efficiency following pressed BC-CCDs capacitors on ency to operate the channel between anneal CCD by tion a that least complete This Nuclear Measurements both surface- and buried-N-channel CCDs continue to operate following 10^6 Rad dose at 80K; however, degradation of charge transfer efficiency is much worse in the surface-channel CCD compared to the buried-channel CCD. Experimental data on MNOS capacitors and BC-CCDs shows that the decrease in the SC-CCD transfer efficiency following irradiation at 80K is not caused by radiation-induced interface states. A proposed model of charge buildup in the integrate oxide is consistent with observed CCD behavior and is supported by experimental data on the dependence of transfer efficiency on clock voltage swing.

Measurements of the interface state density in capacitors and BC-CCDs show that interface state formation by ionizing radiation is almost completely suppressed at 80K. The increase in Dit observed in a BC-CCD irradiated at 10^6 Rad Si at 80K is only 1.7x10^{11}/cm^2-eV compared to an expected value of at least 3x10^{11}/cm^2-eV at 295K. Annealing data suggests that temperatures below 100K are required to obtain complete suppression of interface state formation.

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REFERENCES