a test setup. Ground currents can slow the settling time of voltage steps applied to a test circuit or the output voltage to be measured.

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Reference Waveform Flat Pulse Generator

JAMES R. ANDREWS, SENIOR MEMBER, IEEE, BARRY A. BELL, MEMBER, IEEE, NORRIS S. NAHMAN, FELLOW, IEEE, AND EUGENE E. BALDWIN, MEMBER, IEEE

Abstract—The NBS Reference Flat Pulse Generator (RFPG) is used to transfer dc voltage and resistance standards to the nanosecond domain. It provides a step amplitude of 1.000 V (open circuit) from a source impedance of 50.0 Ω. The transition duration is 600 ps, and all perturbations are damped out to less than ±10 mV within 5 ns. It can also be used as a time interval transfer standard.

INTRODUCTION

The need for a reference step-like generator has become increasingly important for accurately characterizing the step response of oscilloscopes, transient recorders, and fast sampling channels of digital measurement instruments and automatic test equipment (ATE). By comparing the measurement waveforms and/or data with those of a reference waveform, the fidelity with which the measurement system can acquire the waveform can be determined. The dynamic performance of a measurement system is often desired, together with its ability to measure dc or steady-state quantities.

From a practical point of view, it is often desirable to be able to calibrate the dc voltage levels of the measurement system, as well as any time-dependent parameters. For this reason a voltage step function, whose beginning and ending dc levels are calibratable, has considerable merit as a reference standard, particularly if the transition between these two levels is also well behaved and predictable. Such was the purpose for developing the Reference Flat Pulse Generator (RFPG) at NBS.

AVAILABLE WAVEFORM

In theoretical time-domain studies the ideal unit step generator is commonly used as a driving source. However, in experimental work the ideal generator must be replaced by a physically realizable one, i.e., a step-like transition generator.

The voltage step-like transition generator produces a non-instantaneous voltage transition from an initial voltage level to a final one. An equivalent circuit for the voltage transition generator may be characterized in terms of the step response $E_S(s)$ of a four-terminal network having a voltage transfer

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problem stems from the use of transmission lines in the typical mercury switch pulse generator design. The skin effect losses in the coaxial cable charge line cause a definite distortion of the pulse topline.

Commercial tunnel diode pulse generators exist with transition durations of the order of 20 ps. These generators provide extremely fast transitions but exhibit some waveform distortions due to trigger ramp, etc. The cleanest commercial TD step generator was described in detail by George Frye at the 1968 CPEM Conference [3]. The major limitation in using tunnel diodes is the long-term sag in their output voltage due to internal heating of the junction [3]. Thus they cannot be used for accurate calibration transfer from dc.

Other examples of reference waveform generators are the NBS reference waveform generators based upon transmission line dielectric loss produced by liquid dielectrics exhibiting a Debye relaxation process [1], [4], [5]. These generators employ dielectric loss to realize uniform transmission line filters. The filters provide a reflection-free low-pass bandwidth limiting process and, in turn, a Gaussian-like transition waveform upon being driven by a tunnel diode transition generator. Using a tunnel diode transition generator having about a 20-ps transition duration, three filter assemblies provide available waveforms having 50-, 100-, and 200-ps transition durations across a 50-Ω load. These generators can be used to evaluate the high-speed, leading-edge transient performance of oscilloscopes and other waveform recording devices.

**Flat Pulse Generator Concept**

A flat pulse generator is needed to bridge the gap between dc voltage standards and the extremely fast transient generators such as tunnel diodes. In 1971, Andrews proposed and built a simple circuit which showed that it would be possible to build a generator to transfer dc voltage to the nanosecond region. The simple block diagram shown in Fig. 3 illustrates the principle.

Assume the load \( R_l \) is disconnected. Initially, the switch \( S1 \) is open. Current \( I_{dc} \) from the current source flows through the ideal diode \( CR1 \) and the resistor \( R_g \). Thus the open circuit voltage developed across the output terminals is simply \( V_{dc} = I_{dc} \times R_g \). The output impedance \( Z_g \), seen looking back into the output terminals, is simply \( R_g \) since a current source, by definition, is an infinite impedance. Now at \( t = t_0 \), the switch closes. The anode of diode \( CR1 \) is pulled down to \(-V\). The diode is now reverse biased and ceases to conduct, thus disconnecting the output from the current source and the switch. All of the current \( I_{dc} \) now passes through the switch to \(-V\). The open circuit output voltage is now precisely 0 V. The output impedance is still \( R_g \). Thus we have a generator which switches between two known output voltages (\( I_{dc} \times R_g \) and 0 V) with a constant output impedance \( R_g \).

In 1981, NBS built a prototype RFPG implementing the above concept. Fig. 4 shows the basic schematic diagram for the output stage of the RFPG. Q4 functions as the dc current source \( I_{dc} \). Q2 is the switch \( S1 \). Q1 and Q2 form an emitter-coupled, differential switch pair. They are driven in push–pull by the complementary outputs of an ECL gate. Q3 is the
current source for the emitters of \( Q_1 \) and \( Q_2 \). \( I_e \) must be greater than \( I_{dc} \). Initially the base of \( Q_1 \) is an ECL "1" (-0.9 V) and the base of \( Q_2 \) is an ECL "0" (-1.7 V). Thus \( Q_2 \) is off and \( Q_1 \) is on, conducting all the emitter current \( I_e \) to ground. The current \( I_{dc} \) from \( Q_4 \) all passes through \( CR_1 \) to \( R_g \) creating an open circuit output of 1.00 V (20.0 mA \( \times \) 50.0 \( \Omega \)). \( CR_1 \) is conducting while \( CR_2 \) is reverse biased and nonconducting. At \( t = t_0 \) the input to the ECL gate is switched. The ECL complementary outputs rapidly switch \( Q_1 \) off and \( Q_2 \) on. \( Q_2 \) now conducts all of the 30-mA emitter current \( I_e \). Thus the collector of \( Q_2 \) tries to pull 30 mA from the node connecting \( CR_1, CR_2, Q_2, \) and \( Q_4 \). The only way for the nodal currents to balance is for \( Q_4 \) to supply 20 mA, \( CR_1 \) to become nonconducting, and \( CR_2 \) to turn on and supply 10 mA. Hence, we have accomplished the desired function of turning off \( CR_1 \) and disconnecting \( I_{dc} \) from the output. In actual practice, only the negative going transition from 1 to 0 V is considered as the reference step transition. It is far easier to control the transient behavior by turning off \( CR_1 \) than when turning it back on.

**NBS RFPG**

The NBS RFPG is shown in Fig. 5. Fig. 6 shows the reference transition waveform, i.e., the observed waveform across a 50-\( \Omega \) load, as observed on a sampling oscilloscope. The output transition waveform into 50 \( \Omega \) is a negative going step from 500 mV (1.000-V open circuit) to 0.000 V with a 90- to 10-percent transition duration of approximately 600 ps. As can be seen, the baseline perturbations damp out rapidly.

The RFPG was also designed to be used as a transfer standard for time interval measurements. To accomplish this, all of the timing functions are obtained by digitally counting discrete clock cycles of an internal 10-MHz crystal oscillator. ECL integrated circuits are used exclusively to maintain low timing jitter. The main output pulse and the trigger output pulse come from identical output stages and have identical waveforms. The repetition rate can be set to 1 MHz, 100 kHz, 10 kHz, or 1 kHz. The duty cycle is fixed at 10 percent for the main pulse and 50 percent for the trigger pulse. The trigger-to-pulse delay is selectable at either 0 ns, 100 ns, 200 ns, or 300 ns. The jitter in the delay is 25 ps or less. A mode control sets the outputs to either high dc (1.000 V), low dc (0.000 V), or pulse. The RFPG is built as a single wide plug-in to be operated in a Tek TM-501 main frame.

The RFPG is calibrated by using primary lab standards of dc voltage, resistance, and frequency. The transition shape and baseline perturbations of the waveform are calibrated using appropriate measurements, modeling, and computer simulation. It is most important to determine the node voltage \( V_1 \) as a function of time, Fig. 4, and the effects of the nonideal diode

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1 This item of commercial equipment is identified in this paper in order to specify adequately the experimental procedure. This identification does not imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the equipment identified is necessarily the best available for the purpose.
CR1 in disconnecting V1 from the output. V1 can be determined by either time domain measurements, Fig. 7, or computer simulation of the output stage. The major diode effects that must be considered are: 1) nonlinear I-V characteristic; 2) nonlinear C-V characteristic; and 3) charge storage-recovery transient effects. The charge storage effects are minimized by using a high-speed Schottky diode. The output baseline perturbations are primarily due to the driving node waveform V1 being capacitively coupled to the output via the reverse-biased diode CR1.

MODELING AND COMPUTER SIMULATION

The motivation for doing computer analysis and simulation of the RFPG is that in order to have a waveform generator standard, one needs a theoretical basis for how the electronics generate the various electrical waveforms. Circuit modeling, using known or measured parameters for the circuit model, allows one to approximate the actual results and thereby predict the circuit performance from basic principles, which in turn, yields the available waveform.

The circuit analysis programs developed for the RFPG were written using super-SCEPTRE. Waveform generation by computer simulation of the RFPG was conveniently obtained by accessing via a graphics terminal over a multiplexed hardwired link at 9600 baud.

For the purpose of modeling the RFPG, the ability to utilize time-dependent, nonlinear circuit elements provided for in SCEPTRE was essential [6]. In particular, primary dependent current sources for ideal diodes proved to be especially convenient when combined with voltage- or current-dependent capacitors. Secondary dependent current sources with nonlinear, table-entered dependencies permitted the development of an accurate model for the RF-switching transistors used in the output stage of the RFPG.

The output stage of the RFPG consists of positive and negative current sources that are steered by means of transistor switches. An initial model that was used for simulating the output stage is shown in Fig. 8. The output diode (CR1) can be simulated by ideal diode current JD1 and associated components C1, L1, C4 and, together with load resistor R3, form the output branch of the generator circuit. Similarly, JD2, C2, L2, and C5 represent the reverse clamping diode (CR2) connected to driving node 4. C1 and C2 are voltage-dependent junction capacitances, L1 and L2 are package inductances, and C4 and C5 are the package capacitances of the respective diodes. R2 and C3 are the filter components for controlling part of the undershoot contained in the negative going transition of the output waveform. J1 and J2 are the nominal 20-mA and 30-mA positive and negative constant current sources. To simulate the action of the switching transistors, time-dependent resistors R1T and R2T are utilized. The resulting driving node and output voltage waveforms obtained from this initial model reveal that the actual step-like output waveform is limited by the speed of the transistor switches more than by the properties of the output current-steering diodes.

Fig. 9 shows a simple common-emitter equivalent circuit that was developed for the RF switching transistors, based on a modified Geller, Mantek, and Boyle (GMB) model [7]. The primary difficulty overcome with the use of this model is the effect of the nonlinear base-to-emitter characteristics of the transistor when driven with large signals having low source impedances. The basic GMB model represents the base-emitter junction (from charge control theory) as the nonlinear forward resistance of a diode in parallel with a current-dependent capacitor. An analysis which supports this modified GMB model can be made by noting that for the forward-biased base-emitter junction

\[
I_{b'e} = I_0 \left[ -1 + e^{\frac{e}{kT}(V_{b'e} - E_3)} \right] \tag{3}
\]

so that

\[
[r_{b'e}] = \frac{dI_{b'e}}{dV_{b'e}} = \frac{e}{kT} (I_{b'e} + I_0) \tag{4}
\]

where \(e/kT = 38.7\) at \(T = 300\) K, \(I_0\) is the base-emitter reverse saturation current, and \(E_3\) is an offset voltage in the base-emitter I-V characteristic.

It is well known that when the junction transition is switched by means of a large step of base current but does not saturate, the collector current is approximately an exponential function of time [8]. The nonlinear GMB model shown in Fig. 9 simulates this type of response by means of the time constant, \(T_{b'} = r_{b'e}C_1\), which is considered to be invariant over the entire base current excursion. Consequently, \(C_1\) is seen to be a function of the nonlinear base-emitter current, since

\[
C_1 = \frac{T_{b'}}{r_{b'e}} = \frac{eT_{b'}}{kT} (I_{b'e} + I_0). \tag{5}
\]

The general expression for the static base-emitter I-V characteristic is given by

\[
V_{be} = I_br_{bb'} + V_{D1} + E_3 \tag{6}
\]

where

\[
V_{D1} = \frac{kT}{e} \ln \left( \frac{I_b}{I_0} + 1 \right) \tag{7}
\]

is the ideal diode voltage, and the \(J_1\) current source (leakage current of the back-biased collector-base junction) is neglected. Consequently, the bulk resistance \(r_{bb'}\) can be found by rearranging (6) and using (7) to give

\[
R_1 = r_{bb'} = \frac{1}{I_b} \left[ V_{be} - E_3 - \frac{kT}{e} \ln \left( \frac{I_b}{I_0} + 1 \right) \right]. \tag{8}
\]
The remaining elements of the model are the conventional hybrid circuit components, except that \( J_2 \) is not simply beta (or \( \alpha_{fe} \)) times the base current. Rather, the beta variation with current level is accounted for by means of tabular data. \( R_2 \) is the saturation resistance of the collector characteristic.

Finally, the modified GMB model for the transistors, together with appropriate ECL input drive signals, is used to replace the \( R_{1T} - R_{2T} \) resistors in the basic output stage model of Fig. 8. The use of a more complete model is then possible for investigating the effects of parameter variations on the RFPG output waveform simulation. Fig. 10 shows an example of the available transition waveform across a 50-\( \Omega \) load of the
RFPG produced by computer simulation (c.f. Fig. 6). Fig. 11 shows a similar example of the corresponding driving node voltage $V_1$ obtained (c.f. Fig. 7) [9].

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