A Sensitive Analog Comparator

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Abstract—A strobed, sensitive analog comparator has been developed for use in the NBS Data Converter Test Facility. The comparator has a sensitivity of 1.5 μV and a response time of 30 μs to within 10 μV, following input steps up to 20 V. Signal voltages up to ±10 V are compared with reference voltage levels of opposite polarity, using a precision resistive divider. The input offset has a temperature coefficient of −1 μV/°C and changes less than ±5 μV under worst case dynamic conditions. Following a strobe pulse, the digital output is retained until the next strobe pulse. Optical isolators provide isolation between the analog and digital circuits.

Key Words—Analog comparator; comparator; overdrive; settling time measurements; strobed comparator; voltage comparator; voltage limiting.

I. INTRODUCTION

A SENSITIVE analog comparator was required for use with an 18-bit D/A converter standard to provide a simulated, 18-bit A/D converter (ADC) check standard for the National Bureau of Standards (NBS) Data Converter Test Facility [1], [2]. The check standard serves as an independent means for verifying the accuracy with which code transition levels (0- to ±10-V range) are measured, when the facility is operating in the ADC mode.

The performance characteristics required for the comparator included a settling time of 30 μs to within 10 μV (following input steps up to 20 V), a linearity error of less than 1 ppm between input signal and reference voltages, and less than 10-μV change in input offset voltage under worst case dynamic conditions. Since a comparator with these characteristics was not available, one was developed having the following performance specifications:

Input range (signal or reference): ±10 V.
Input impedance (signal or reference): 5 kΩ.
Input sensitivity: 1.5 μV.
Linearity error (signal versus reference): Adjustable to zero; less than ±5-μV change under worst case dynamic conditions; temperature coefficient, —1.1 μV/°C.
Response (settling) time: 30 μs to within a settling error of 10 μV, following input steps up to 20 V.\(^1\)
Noise: 8 μV rms, referred to input.
Digital circuits: Following a strobe pulse, the digital output is retained until the next strobe pulse. Optical isolators provide isolation between the analog and digital circuits.

II. GENERAL DESCRIPTION

A simplified diagram of the sensitive analog comparator is shown in Fig. 1. To facilitate very accurate measurement of large signals, i.e., voltages ranging up to ±10 V, a precision resistive divider \((R1, R2)\) is utilized to compare the signal levels \(V_s\) with reference voltage levels \(V_R\) of the same nominal values, but of opposite polarity. The amplifier/limiter (AL), connected to the center tap of the divider, amplifies the algebraic sum of the signal and reference levels by a factor of 100 and applies the amplified signal to the positive input terminal of a commercial differential analog comparator (CP). This unit has an input uncertainty band, after the offset voltage has been nulled, of about ±150 μV. This uncertainty corresponds to ±1.5 μV, referred to either the signal or reference input, and

\(^1\) Settling error includes input sensitivity.

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is designated “input sensitivity” in the performance specifications. The gain factor of 100 only applies to small values of $|V_S + V_R|$; large values are limited and amplified by smaller factors to minimize settling time problems. Slow voltage offset drift in AL is compensated by the chopper stabilized amplifier, CSA, whose output is applied via $R_4$ to the negative input terminal of CP. The “comparison level” control is used to adjust the threshold level of the CP. Filter $R_3-C$ serves to reduce the noise in the output signal of AL.

Input strobe pulses to the comparator are applied via an optoisolator and monostable multivibrator (for producing a standard strobe pulse length). Outputs from CP, present only when the latter is strobed, are stored in a bistable latch and fed to the output via an optoisolator. These optical couplers isolate the digital circuits from the analog circuits and are required to minimize ground currents, which distort and offset the analog signals.

The analog circuits of Fig. 1 required the most design consideration, particularly those affecting the settling time, input offset, linearity, and noise specifications. These specifications and the circuits employed to meet them are discussed in the next section.

III. DESCRIPTION OF ANALOG CIRCUITS

A. Linearity

The linearity error between signal input and reference voltages is determined by variations in the $R_1/R_2$ ratio caused by room-temperature variation and possible unequal self-heating of $R_1$ and $R_2$. The room-temperature effects are held to the specified value by matching the temperature coefficients of $R_1$ and $R_2$ to within 0.2 ppm/°C. Unequal self-heating of $R_1$ and $R_2$ results if the integrals of $V_R$ and $V_S$ differ appreciably over time intervals which are not significantly shorter than the thermal time constants of the resistors. To meet the self-heating specification (under worst-case dynamic conditions), resistors were used with temperature coefficients of less than ±0.6 ppm/°C, and having estimated temperature rises of only 0.5°C with 10 V applied (20-mW dissipation). Thus with 10 V applied to one resistor and 0 V to the other, the maximum change in $R_1/R_2$ is 0.3 ppm.

B. Settling Time

The settling time of CP (<0.1 μs) is negligible compared with the settling time of the sensitive comparator; therefore, the latter is determined entirely by the combined response of amplifier/limiter AL and the noise filter $R_3-C$. The maximum acceptable settling error is 10 μV after a settling time of 30 μs. Since the input sensitivity is 1.5 μV, the combination of AL and the filter must settle to within 8.5 μV in 30 μs. This settling error corresponds to an error of 0.85 mV at the outputs of AL and the filter, because the gain from the signal input to these points is 100. It is important to minimize the settling time of AL, so that the time constant of $R_3-C$ can be made as large as possible (for maximum noise filtering) within the settling time constraint.

Fig. 2 is a detailed diagram of the analog section of the comparator. Note that the amplifier/limiter AL shown in Fig. 1 consists of signal amplifiers $AR_2$ and $AR_3$, and the limiting amplifier $AR_1$. These amplifiers are of a commercial type which has a unity gain bandwidth of 15 MHz and a unity gain settling time of 500 ns to within 0.01 percent of full scale. Factors which may increase the settling time of an amplifier are dielectric absorption of internal capacitors, thermal transients (self-heating effects), limited slew rate, and certain linear effects [3]. Because of these factors, settling time is usually not specified in terms of a settling error smaller than 100 ppm of full scale. Regardless of which factors are affecting an amplifier’s response, settling time to within a given settling error can usually be minimized by limiting the voltage and current excursions as much as possible in the various stages of the amplifier. The maximum required input-voltage range of the differential comparator CP is ±3 mV, including offset voltage; hence, there is no practical restriction on the limiting imposed on the signals applied to $AR_2$ and in $AR_2$ and $AR_3$.

To minimize the voltage and current signal levels in $AR_2$, it is necessary to limit the voltage levels at node $P$ to small values. Clipping diodes $D_1$ and $D_2$ limit the voltages at nodes $M$ and $P$ to approximately ±0.4 and ±0.18 V, respectively. (Nodes $N$ and $Q$ are held close to 0 V by $AR_1$ and $AR_2$.) Further limiting of $V_P$ is impractical without using active circuits to effectively reduce the forward voltage drops of clipping diodes. Therefore, amplifier $AR_1$ is used to forward bias $D_3$ or $D_4$ (depending upon the polarity of $[V_S + V_R]$) proportionally to the voltage levels at nodes $M$ and $P$. It is seen that, within the bandwidth constraints of $AR_1$, the voltages at nodes $M$ and $P$ are amplified by factors of approximately $R_6/R_4$ and $R_6/R_5$, respectively. Except for transients of approximately 1-μs duration that occur when either input signal or reference voltage steps are applied, limiter $AR_1$ reduces the values of $[V_P]$ as shown in Fig. 3. Diodes $D_5$ and $D_6$ limit the output voltage of $AR_2$ to ±130 mV (excluding transients) and also serve to reduce the amplitude and duration of the switching transients applied to node $Q$. Diodes $D_7$ and $D_8$ in $AR_3$ are used to limit the voltage excursions at node $S$ to the smallest practicable values (approximately ±240 mV). This voltage limiting helps to reduce the settling times of $AR_3$ and noise filter $R_{14-C2}$, designated $R_3-C$ in Fig. 1. All diodes shown in Fig. 2 are high-conductance Schottky types. Diodes $D_5$ through $D_8$ have zero-bias resistances which are sufficiently low (~0.7 MΩ) to affect the gains of $AR_2$ and $AR_3$. 

Fig. 2. Analog section of sensitive comparator.
The test method described in the Appendix was used to measure the settling times at nodes S and W to within a settling error of 0.85 mV. The settling times at node S ranged from 2 to 15 μs, approximately, depending upon the value of |V_S + V_R| before it was switched to zero. The noise filter time constant was selected so that the maximum settling time at node W (analog output) was 30 μs. As mentioned before, this settling time also applies to the sensitive comparator as a whole. When the limiter stage AR1 was disconnected from the circuit, the maximum settling times at nodes S and W increased to approximately 35 and 45 μs, respectively.

C. Input Offset

The chopper-stabilized amplifier, CSA, shown in Figs. 1 and 2 was used primarily to compensate for input offset voltages in AR2 and AR3, resulting from room-temperature changes. CSA will compensate exactly for the offset voltage at node Q if its gain is made equal to the product of the noise gain of AR2 and the signal gain of AR3. The gain was trimmed slightly from this value, however, to compensate for the temperature coefficient of the input offset voltage of AR3.

The changes in offset voltage under dynamic conditions were measured as described in the Appendix and found to be less than ±1 mV at the output of AR3. The compensating output from the CSA effectively reduces this offset to less than ±0.5 mV, which corresponds to ±5 μV at the signal input terminal. The effect of switching transients on CSA was measured using the test setup of Fig. 5. The signal source was adjusted (see Fig. 4) so that |V_m| = 10 V and a = b = 30 μs, thus generating switching transients of maximum size at a maximum rate at node Q. The voltage change observed at the output of CSA was less than 0.2 mV, a negligible amount. Therefore, the integral of the switching transients at node Q is very small.

D. Input Noise

The measured noise at the analog output of the comparator is approximately 0.8 mV rms, or 8 μV, referred to the signal input terminal. To a first approximation, this noise equals $E_N(G_N/G_S)$, where $E_N$ is the input noise voltage of AR1 and $G_N$ and $G_S$ are the noise and input signal gains of the AR1 stage.

The calculated value of $G_N/G_S$ is 3.6. Since each of the input circuits of AR2 (including the CSA stage) contributes to the size of $G_N/G_S$ it is evident that a tradeoff is possible between improved input noise and improved settling time by deleting the AR1 stage. If the AR1 stage is deleted, nodes M and P connected, and R8 decreased for proper AR2 gain, the value of $G_N/G_S$ decreases to 2.5 with a consequent decrease of input noise to approximately 5.5 μV.

Although the comparator noise should be minimal, this is not critical, since the NBS Converter Test Set averages the data from 166 successive measurements for each calibration point. This data averaging effectively reduces the comparator rms noise to less than 1 μV.

IV. Summary

A strobed, sensitive analog comparator has been developed by combining a comparison amplifier with a commercial differential voltage comparator (CP). The comparison amplifier basically consists of a precision voltage divider for comparing input signals $V_S$, up to ±10 V, with reference voltages $V_R$ of opposite polarity; a voltage limiter; and a signal amplifier that is drift-compensated by a chopper-stabilized amplifier (CSA). Very small values of |$V_S + V_R$| are amplified by a factor of 100 and applied to one input of CP. Input voltage offset in the signal amplifier is amplified by CSA and applied to the other input of CP. This action compensates for the offset of room-temperature change to within 1 ppm/°C and for offset change, under worst case dynamic conditions, to within 0.25 ppm. Resistors with very low, matched temperature coefficients are used for the voltage divider so that nonlinear effects from ±1°C room temperature variation and maximum differential self-heating of the resistors does not exceed 0.6 ppm.

To minimize the settling time of the signal amplifier, extensive limiting of |$V_S + V_R$| is employed, since the latter can be as large as 20 V before switching to ~0 V. An active voltage limiter and Schottky clipping diodes are used to limit the voltage levels applied to the signal amplifier to less than 6 mV. Also, clipping diodes are used in the feedback loops of the amplifier to reduce the signal levels. Use of the active voltage limiter reduces the maximum settling time of the signal amplifier output from 35 to 15 μs. The decreased settling time was sought, since it allows for a considerable amount of noise filtering after the signal amplifier without exceeding the required settling time of 30 μs. Settling times were measured under a wide range of dynamic conditions (see Appendix) to within a very small settling error, 0.43 ppm of full-scale input. Previously, the smallest settling error used in settling time measurements was 2 ppm, applicable to 18-bit D/A converters.

APPENDIX

The analog section of the comparator was tested with the signal and reference inputs connected together and switched between selected levels $V_m$ (ranging up to ±10 V) and 0 V with various duty cycles $a/(a + b)$ as shown in Fig. 4. The settling time and offset were measured during the transition from $V_m$ to 0 V. The test was implemented using the test circuit shown in Fig. 5 and employed an oscilloscope with a differential vertical amplifier to observe the waveforms at the ANALOG OUTPUT terminals. Diode D of the signal source is used to “disconnect” the pulse generator from resistor
Fig. 4. The analog section of the comparator was tested as shown in Fig. 5 with $V_S$ and $V_R$ equal and switched between selected levels $V_m$ and 0 V with various duty cycles $a/(a+b)$. Offset and settling time of comparator’s analog output were measured during time interval $b$.

![Diagram of analog section](image1)

Fig. 5. Dynamic test circuit for analog section of comparator. Diode terminals are reversed for negative test pulses.

A vertical amplifier sensitivity of 5 mV/cm was usually employed to measure settling times and voltage offsets. Thus a deflection of 2 mm (representing 1 mV) corresponded to 10 μV, referred to the signal input. Since the maximum output from $AR3$ of ±240 mV represented a considerable overdrive of the oscilloscope’s vertical amplifier, it was necessary to determine whether the oscilloscope was contributing to the measured settling times and voltage offsets. This was accomplished by applying voltage waveforms to the oscilloscope which simulated the output from $AR3$ during tests but were obtained directly from the signal source in Fig. 5. These tests indicated that the recovery “tails” following 240-mV pulses were sufficiently short to be ignored in the comparator settling time measurements. On the other hand, oscilloscope offsets were not negligible. These offsets ranged up to ±0.8 mV and were applied as corrections to the comparator offset measurements.

REFERENCES


Effect of Shielded Room on Standard Magnetic Field

HIROSHI NAKANE, HITOSHI MARUYAMA, SHUNICHI OMORI, MEMBER, IEEE, AND ICHIRO YOKOSHIMA

Abstract—The near-zone magnetic field generated by a small loop antenna has been used for sensitivity test of a radio receiver. When external interference fields exist around the antennas, the test must be carried out in a shielded room. The formulas to estimate the effect of the shielded room on the standard magnetic field are derived for the coaxial and the coplanar alignments of the loops. The differences between the values calculated from the formulas and measured ones were within ±0.15 dB up to 50 MHz.

INTRODUCTION

The NEAR-ZONE magnetic field radiated by a small loop antenna has been used for the sensitivity test of receivers with loops [1]. The theory to estimate the standard magnetic field can be applied only in free space. In order to avoid the external interference field, the test has often been carried out in a shielded room. As the magnetic field strength incident on the receiving loop in the shielded room differs from the one in free space by some amount of additional magnetic field due to the presence of the room, it is necessary to estimate the effect of the shielded room on the magnetic field strength. The radiating and receiving loops are usually located in coaxial [1] or coplane [2] to each other in the room. Al-