A Bridge Circuit for the Dynamic Characterization of Sample/Hold Amplifiers

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Abstract—A transformer bridge technique is described for measuring the dynamic performance of sample/hold amplifiers (S/H's). The technique accurately measures dynamic gain errors, signal delay, aperture time delay and jitter, and acquisition time. These parameters are of particular importance to simultaneous data acquisition. The bridge is self-calibrating, and the voltage and time resolution are primarily limited only by the oscilloscope which serves as a detector.

I. INTRODUCTION

SAMPLE/HOLD amplifiers (S/H's) are frequently used in simultaneous data-acquisition systems in which two or more analogue input channels must be sampled at precisely the same points in time; in some systems these sampling instants must be accurately correlated in time with the input signal waveform. Information for determining the degree to which S/H's can perform these functions is generally not available from manufacturers' data sheets, and little attention has been paid in the literature to measurement techniques appropriate for these conditions. A transformer-bridge circuit has been investigated which is capable of providing the necessary information.

A number of terms will be used in the following discussion, and because of the lack of standardized terminology in the industry, the intended definitions are presented here.

Dynamic Gain Error: real (in-phase) component of the expression \((V_{\text{out}} - V_{\text{in}})/V_{\text{in}}\), measured in the tracking (sampling) mode, with sinusoidal input.

Signal Delay: imaginary (quadrature) component of the above expression, i.e., the delay time between input and output.

Sample Time Delay: delay of the S/H response to the hold command, i.e., the time interval between the hold command and the effective instant at which holding begins.

Aperture Time Delay: net time interval by which the effective sampling instant (on the input waveform) is delayed (or advanced) with respect to the application of the hold command. (This interval has two components, one due to the signal delay through the S/H circuit and another due to the delayed response of the circuit to the hold command— the sample time delay.)

Aperture Delay Jitter: uncertainty in the aperture time delay due to jitter internal to the S/H itself.

S/H Offset: permanent jump in the output voltage at the moment of hold.

Acquisition Time: maximum time after application of the sample command required for a S/H to begin tracking an input signal within a specified error band.

For an ideal S/H circuit having a cutoff frequency \(f_c\) and a single-pole frequency response, the complex gain error at frequency \(f\) is given by

\[
\varepsilon = \frac{V_{\text{out}} - V_{\text{in}}}{V_{\text{in}}} = -j\frac{f}{f_c} + j\frac{f}{f_c^2} < 1.
\]

The first term, the dynamic gain error, increases very slowly until the cutoff frequency is approached, whereas the second term, the signal delay, is directly proportional to the frequency. For simultaneous sampling and/or time correlated sampling applications, both of these terms should be determined. Furthermore, in actual practice, additional poles may exist in the transfer function altering the error expression and making actual measurements of the errors especially important. Additional timing errors associated with the holding function, are equally important and also must be determined.

II. THE BRIDGE CIRCUIT

The circuit, presented in Fig. 1, is a transformer-ratio-arm bridge adapted to measure, in conjunction with a wide-band differential input oscilloscope, the quantities defined above. The measurements are made by inserting the S/H under test in one arm of the balanced bridge such that the tracking output supplies the voltage across that arm. The S/H dynamic gain error and signal delay cause the bridge to become unbalanced, and upon rebalancing, the changes in the bridge's magnitude \(T_1\) and phase components \(T_2\) provide a direct measure of these errors. Unbalanced residues resulting from harmonic distortion are observed directly on the oscilloscope. Since the S/H can be removed and the bridge rebalanced, the circuit is self-calibrating. The bridge balance equations, ignoring terms of second and higher order, are as follows.

Dynamic Gain Error:

\[
\varepsilon = 4(\rho_{e2} - \rho_{e1})
\]
where \( \rho_{t2} \) and \( \rho_{t1} \) are the settings of \( T_3 \) for the test and self-calibration balances, respectively.

**Signal Delay:**

\[
\tau = 4R_1C_3(\rho_{t2} - \rho_{t1})
\]

where \( R_1C_3 \) is the time constant of the phase balancing network, \( \rho_{t2} \) and \( \rho_{t1} \) are the settings of \( T_3 \) for the test and self-calibration balances, respectively, and \( T_2 \) has a ratio of 1/1.

Transformers \( T_1 \) and \( T_4 \) are of in-house construction. Their principal function is to provide isolation, and high accuracy is not required. \( T_1 \) is also used to double the output voltage from the signal generator. Transformers \( T_2 \) and \( T_3 \) are, respectively, 4- and 6-dial commercial audio-frequency inductive voltage dividers. The first, \( T_2 \), serves the dual functions of splitting the input signal into two nearly equal complementary signals and providing the phase balance; the second, \( T_3 \), forms the primary adjustable bridge arms. By establishing the bridge common at \( T_2 \), loading errors on \( T_3 \) are eliminated. Further, any small unbalance due to the common return through the output impedance of \( T_2 \) is reduced by the common mode rejection of the oscilloscope's input amplifier.

It should be noted that an accurately balanced bridge can nevertheless give erroneous readings if the common-mode voltage approaches the voltage across either of the bridge arms when the setting of \( T_3 \) deviates appreciably from 0.5. Whereas the S/H output voltage is referred to ground, the bridge balance is referred to the virtual ground, and resulting second-order error terms could become significant. The low output impedance (\(<5 + j5 \Omega\)) of inductive dividers normally renders this error insignificant.

For the very high frequency components of the S/H output produced during mode changing, the bypass capacitors \( C_1 \) and \( C_2 \) maintain a low-impedance path to ground. To avoid ringing, small series damping resistors are added.

Resistors \( R_2 \) and \( R_3 \) are nominally 1 k\( \Omega \) each and are selected for very low, matched time constants. Resistance matching itself is not critical since the bridge is self-calibrating. The phase balancing network components \( R_1 \) and \( C_3 \) are chosen to have a negligible phase error \((\omega R_1 C_3)\) at the maximum frequency of interest. If greater measuring range is required than this expression permits, the ratio of transformer \( T_4 \) can be increased.

Table I gives typical bridge self-calibration data for frequencies up to 100 kHz, using a commercial high-audio-frequency divider for \( T_3 \). These bridge corrections are estimated to be accurate to within \(+ (10^{-5} + 10^{-8} f^2)\), where \( f \) is the signal frequency in kilohertz. The corrections for \( \tau \) are considered accurate to \(+ 0.2 \text{ ns}\). Future improvements may be possible using more sophisticated inductive divider techniques which have recently been described. These are capable of considerably higher accuracy at frequencies up to 1 MHz [1], [2].

### III. Aperture Time Delay Measurement

To observe in detail the S/H performance as the mode is switched between track and hold, the test unit is commanded to hold for a period during each cycle of the input signal. If the bridge is balanced, the waveforms of Fig. 2 are observed in which the balance condition is interrupted only during the hold period. Either of the two transitions can be investigated in detail by expanding the oscilloscope time base.

The balanced bridge is an ideal starting point from which to measure the aperture time delay, since the conditions are well known up until the moment of hold and jitter between the hold command and the input waveform causes negligible uncertainty to the first order. After the hold condition

![Fig. 1. The basic S/H bridge circuit.](image)
begins, the displayed bridge output indicates the reference waveform slewing offscale, with the S/H switching and settling transients superimposed. A triangular input waveform, having a slope of $K \text{ V/s}$, provides a useful reference for this measurement, since the bridge output will change at one-half the same constant rate after the S/H settles. By extrapolating back to the point of intersection with the balanced output, the effective sample time delay can be found, i.e., the time delay between the hold command and the point of intersection. This point can be readily located (even in the presence of a S/H offset), by free running the signal generator with respect to the mode control. The resulting bridge output sweeps through consecutive positive and negative ramps, giving an expanded trace as shown in Fig. 3(a).

Disconnecting the phase balancing circuit will offset the bridge balance by $V = KT$ (peak to peak) and advance the point of extrapolated intersection back in time to the actual sampling instant as shown in Fig. 3(b). The aperture time delay is then the time interval between the initiation of the hold command and the actual sampling instant. This measurement permits accurate correlation between the hold command and the actual point being sampled on the input waveform. The accuracy of this aperture-time-delay measurement is determined largely by the minimum required horizontal deflection factor and the minimum resultant time resolution. This factor, in turn, is dependent upon the S/H settling time, since the settled waveform must be displayed. In practice, these conditions place an accuracy limit of approximately 20 ns on the measurement. This uncertainty can be reduced by nearly an order of magnitude, if required, by the following method which is minimally dependent on the accuracy of the oscilloscope.

By adjusting the phase balance $\rho_r$ to some new value $\tau'$ greater than the actual signal delay, it is possible to retard the point of intersection of the bridge waveforms to a point beyond the settling time, as shown in Fig. 4. This time delay, of course, is readily calculated from the setting $\rho_r$. The intersection point can then be displayed with any desired horizontal deflection factor by accurately delaying the oscilloscope trigger pulse. This delay is accomplished with a selectable digital delay whose input is derived from the hold command. The digital delay $t_d$ and the signal delay setting $\tau'$ can be set to position the point of intersection at a precalibrated coordinate on the oscilloscope. The aperture time delay is now given solely in terms of the values of $\tau'$ and $t_d$, as $t_d - \tau'$. The measurement is illustrated in Figs. 4 and 5.

In this case, the oscilloscope is used only as a crossing detector. The actual timing accuracy is dependent on the following:

1) the digital delay timing error,
2) the signal delay network error (note that $\tau'$ can be calibrated against the digital delay),
3) the signal delays introduced by the coaxial leads connecting the various components of the test system, and particularly, the delay caused by the oscilloscope's input capacitance and the equivalent bridge source resistance (these can be calculated and/or measured by various substitution methods), and
4) the residual local nonlinearity of the tracking output and reference waveforms, or local differences in slope between the two. Errors in either of these may introduce equal errors in the crossing time measurement.

As an example of 4), if, after time $\tau' = 300 \text{ ns}$, the S/H output has settled to within $1 \text{ mV}$ of the final value and the reference waveform has a constant slope during this time of
The crossing time measurement $t_d$ then will be in error to the first approximation by the same amount for $t_d \approx \tau$. Thus the timing error $\Delta t_d \approx 3 \cdot 10^{-7} \cdot 3.3 \cdot 10^{-3} \approx 1 \cdot 10^{-9}$ s.

In the present test system, the root sum of squares of these errors is estimated to be 4 ns. For applications in which only relative measurements between S/H's are important, the estimated error is 1 ns. For aperture delay/jitter measurements, the primary limitation is the oscilloscope's trigger jitter.

**IV. ACQUISITION TIME MEASUREMENT**

Acquisition time is measured by observing the bridge balance settling time following the application of the track command. Fig. 6 illustrates a S/H settling to within 0.01 percent (of 10-V full scale) in less than 1 $\mu$s. The position and duration of the hold command can be set to produce any desired hold-to-sample voltage excursion, e.g., minus full scale to plus full scale. To reduce the severity of oscilloscope input amplifier overload occurring at high gain settings during the hold mode, the voltage at the node joining $R_2$ and $R_3$ is diode limited. For low repetition rates, this overload is unlikely to affect the aperture time delay measurements described earlier, since the overload occurs after the transition in question. If, however, the subsequent overload affects the acquisition time measurement, a diode-bridge gating circuit can be used to isolate the oscilloscope during the period which would otherwise cause saturation.

**V. CONCLUSION**

A flexible bridge method has been investigated which is capable of providing accurate measurements of a number of important dynamic S/H parameters. Taken together, they define the exact points in time at which the input waveform is being sampled and describe the amplitude accuracy with which these samples are taken. In addition, the measure-
ments determine the time required after digitizing to resample to the desired accuracy. The important parameters which are not determined include the hold-mode droop and feedthrough, both of which can be measured rather easily using straightforward techniques.

A High-Speed Low-Noise 18-Bit Digital-to-Analog Converter

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Abstract—An 18-bit digital-to-analog converter (DAC) with a full-scale current output of 100 mA and a compliance voltage range of ±12 V has been designed for use as a precision voltage output DAC. The output noise and settling time of the new design are considerably lower than obtainable from conventional design approaches. An accurate method of measuring settling time also is described.

I. INTRODUCTION

Programmable voltage levels from −10 to +10 V (approximately) are required to automatically test analog-to-digital and digital-to-analog converters (ADC's and DAC's). In test systems, these analog voltage levels are often supplied by so-called reference DAC's which have at least 4 times the accuracy of the converter under test. However, the time required for the DAC output to settle within 1/2 least significant bit (LSB) of the final value (following an input code change) increases with DAC accuracy. Also, higher accuracy limits the permissible noise level with consequent bandwidth limitation. Thus the natural consequence of increased DAC accuracy is increased settling time. Therefore, it is difficult to obtain reference DAC's with sufficient speed to fully test lower accuracy DAC's and ADC's (e.g., the settling time of DAC's and the effect of conversion rate on ADC accuracy).

At NBS, an 18-bit reference DAC was sought which has sufficient accuracy and speed to dynamically test 15- and 16-bit ADC's and voltage output DAC's. This paper discusses the settling time and noise limitations of high-resolution DAC's of conventional design and proposes an alternate design for an 18-bit DAC to improve these characteristics.

II. GENERAL DESCRIPTION OF DAC'S

DAC's of conventional design may be operated either as current output or voltage output DAC's (current mode or voltage mode of operation). In the current mode, the converter is equivalent to a programmable current source with output current \( I_g \) shunted by a stable resistance \( R_o \) as seen in Fig. 1. For high-resolution DAC's, the full scale range (FSR) of \( I_g \) is limited to about 4 mA and is more commonly 2 mA. Bipolar output results when points a and c are connected. The current source may be shunted by an external resistance to yield a specific output voltage range; however, the maximum range is limited to the "compliance voltage" range, beyond which converter accuracy is degraded. The compliance voltage range is usually less than ±1.2 V for high-resolution DAC's. For voltages within the compliance range, the DAC may be operated in either the current or voltage mode. For larger voltages, the voltage mode must be used. In this mode, points a and b of Fig. 1 are

![Fig. 1. Simplified diagram of conventional DAC. Points a and c are connected for bipolar output, a and b for the voltage mode of operation.](image-url)

REFERENCES


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1 Arbitrarily defined here as 14-bits or more resolution.

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