CMOS IC Stuck-Open Fault Electrical Effects and Design Considerations

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Abstract - The electrical effects of CMOS IC physical defects that caused stuck-open faults are evaluated, including their voltage levels, quiescent power supply current (IDDQ), transient response, and important testing considerations. The transient responses of the defective node voltage and power supply current to the high impedance state caused by a stuck-open defect were measured to determine if the IDDQ measurement technique could detect stuck-open faults. The IDDQ technique does detect stuck-open faults in some designs, but detection is not guaranteed for all circuits. Modifications to the circuit layout to reduce the probability of stuck-open fault occurrence are presented.

I. INTRODUCTION

The stuck-open fault is a failure mechanism associated with loss of charge transfer capability in one or more of the transistors in a CMOS IC logic circuit. This fault causes a high impedance state at the output node for at least one logic state and in such cases the node voltage is assumed to be that of the previous logic state. For example, consider the 2-NOR shown in Fig. 1 which has an open circuit in the drain connection of n-channel transistor MN2. Input condition AB = 01 produces inactivation of MN1 and activation of transistor MN2, but the open circuit prevents active pull-down of the output node. For this condition the output node is in a high impedance state, which may allow the output voltage to remain at the voltage of the previous logic state for some period of time. For this reason, the CMOS stuck-open fault is sometimes referred to as a "memory" fault. As will be shown and discussed later, the occurrence and retention characteristics of memory effects due to stuck-open faults are very dependent upon the electrical characteristics of the defective logic circuit, which can depend upon its local physical structure.

An extensive literature search was performed for information on stuck-open faults; over 125 papers written over the past 13 years were reviewed. The concept of the memory effect of the CMOS stuck-open fault was reported by Case in 1976 [1] and described in more detail by Wadsack in 1978 [2]. A major emphasis since then has been on development of automatic test pattern generation for the CMOS stuck-open fault in combinational logic circuits [2-11]. Detection of the stuck-open fault is made more difficult because certain CMOS circuit configurations introduce hazards due to differential timing delays that can upset the correct initializing pattern [4-11].

Some test patterns that achieve complete logic state testing (or produce 100% of the possible input states) may not detect stuck-open faults. For example, a full binary down-count test vector sequence will not detect the open circuit in Fig. 1. Therefore, the test technique usually considered for the detection of this failure mechanism uses an ordered pair of two test vectors; the first test vector, called an initialization vector (T1), charges the output node to the complementary logic state from that expected when the defective transistor is turned-on. The second vector, called the sensitization vector (T2), is used to evaluate the presence of the stuck-open fault. The T1-T2 sequence for the defect in Fig. 1 is test vector AB = 00 followed by AB = 01. This two vector test sequence depends upon the memory effect to successfully detect the stuck-open fault, but, as previously mentioned, the memory effect is very dependent upon the electrical characteristics of the defective logic.

Fig. 1. 2-NOR logic gate showing an open drain defect location.

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The attempt to detect stuck-open faults in CMOS ICs using special test patterns was reported by Woodhall, et al., in 1987 [12]. They used 6552 test vehicle ICs with 1238 distinguishable single stuck-open sites per die. Fault test sets having 100% coverage were used to determine the presence of stuck-open faults. Forty-four die had one or more stuck-open faults and, of these, 40 die were detected by a stuck-at test set. The stuck-open escape rate using a stuck-at test set with 100% coverage was 0.121% or 1210 parts per million (PPM). The study was reported to have higher defect density than normal due to a contact misalignment problem so the data may have given a pessimistically high estimate of the stuck-open fault escape rate. Also, open circuits were not physically confirmed to exist on the test vehicle ICs. Another study by Turner, et al., reported no stuck-open defects among a sample of SSI and MSI gates; however, the sample size was not given [13]. No publications were found where stuck-open faults were physically described or which had information on actual electrical effects of physical stuck-open faults.

In this paper we describe the functional and parametric effects of physical stuck-open faults in Sandia CMOS 16K ROMs. These defective ICs had open-metal in the drain interconnections of n-MOS transistors located in 2-NOR gates of the address decoders. Two different types of open metal defects were analyzed; one was a relatively large section of missing metal (IC A) and the other was a narrow metal void at a field oxide step in three different 2-NOR decoder gates (IC B). The voltage levels, quiescent power supply current (IDDQ), transient response, and test considerations associated with these defects are reported. The timing relation between the floating node voltage and IDDQ was of particular interest to determine if the stuck-open fault could be detected by a measurement of quiescent power supply current in a production environment [14].

II. METHODS AND RESULTS

The SA3002 is a 2K x 8 fully static CMOS ROM designed by Sandia, which is functionally equivalent to the Intel 8355. The address decoders use the seven least significant bits for row selection and the four most significant bits for column select. Normally, at the beginning of each access cycle, all row decoders are disabled, all bitlines are precharged high, and the 11-bit address is latched on the chip. At the end of the precharge, only one row (wordline), consistent with the latched address, should become active. Under certain conditions, the stuck-open defects described below prevented faulty row decoders from being disabled once they were turned on. Under other conditions, the stuck-open defects allowed the faulty row decoders to drift into the enabled state. Sometimes this caused one row of memory array transistors to remain on during the bit-line precharge or allowed two rows to be on at the same time following precharge.

The first failure condition of IC A was incorrect data from the ROM for certain address sequences. The first failure condition for IC B was occasional high IDDQ following powerup. The measurements that were taken on IC A and IC B are described below.

Measurements on IC A. The stuck-open fault in IC A was caused by the absence of a 10 μm section of metal in the decoder circuitry for memory row 25. Figures 2(a,b) show the normal metal pattern and the defective metal patterning that caused the stuck-open failure mode. The metal is completely missing in a 10 μm long section on top of polysilicon (and intermediate oxide) that ends abruptly at the edges of the polysilicon. Other die from the same wafer lot did not have this defect and no defects were found in the mask. It is believed that the photoresist failed to adhere in this region, resulting in removal of this section of metal during reactive ion etching (RIE) patterning.

Fig. 2(a). Voltage contrast SEM picture of a ROM row decoder 2-NOR circuit showing a normal drain connection. The section where missing metal occurred on the defective 2-NOR gate is indicated.

Fig. 2(b). The 2-NOR gate with a missing drain section.
Fig. 3(a) shows the row decoder subcircuit schematic that includes the defective 2-NOR gate and Fig. 3(b) shows the location of the open metal in the drain interconnect of one of the n-MOS pull-down transistors of the 2-NOR gate. The X|| output (wordline) drives a row of n-channel array transistors whose drains are selectively connected to bit lines.

Fig. 3(a). ROM row decoder subcircuit with the defective 2-NOR gate.

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The transient and steady state voltages of node C of the defective 2-NOR gate could not be probed directly without altering the electrical operation of that node. Therefore, node C was indirectly measured in the high impedance state by placing a 0.5 um metal probe on node VNAND (Fig. 3a) of the 2-NAND gate. Node D was set equal to logic one and the voltage response at node VNAND and the power supply current waveform IDDQ were measured using an HP4145B Semiconductor Parameter Analyzer. The power supply voltage was $V_{DD} = 11$ V, the maximum operating value for which the ROM was designed.

Fig. 4 shows the timing response when node C was driven to a logic low of 0 V ($AB = 11$) prior to setting it in the high impedance state ($AB = 10$). The voltage at node VNAND decayed from 11 V to about 0.4 V over a time period of about 60 s. IDDQ was 147 mA at $AB = 11$ just prior to setting the high impedance state. When $AB$ was then set to the high impedance state ($AB = 10$), IDDQ increased to near 100 mA within an 8 s period and then decreased to about 2 mA over the next approximately 50 s. (Note that $i_D$ will be used to distinguish time-varying power supply current from $i_{DDQ}$, the stable, quiescent power supply current.) The high current peak was interpreted as due to conduction of both the 2-NAND and the large word line driver during the VNAND node high to low transition. The steady

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state voltage at node C during the high impedance state was obtained by placing a second metal probe down at node C and measuring a voltage transfer curve for the 2-NAND gate. The steady state voltage of the floating node was then determined from the transfer curve to be 5.5 V (i.e., approximately VDD/2). The node C voltage of 5.5 V was above the input switching threshold of the 2-NAND, but not high enough to cut off the p-MOSFET. The partially on p-MOSFET in the 2-NAND caused a steady state IDDQ of 2 mA.

Fig. 5 shows the timing response when node C was precharged to a logic high of 11 V (AB - 00) prior to putting it in the high impedance state (AB - 10). VNAND node voltage increased slightly from 0 V to about 0.4 V while IDD increased from 147 nA to about 2 mA. Therefore, it appears that when node C is put in the high impedance state it always drifts to a value near half of the power supply voltage regardless of its initial state.

The steady state IDDQ of 2 mA was caused by a steady state current through the partially on p-MOSFET in the 2-NAND gate since the node voltage was above the input switching threshold of the gate. The node C voltage of 5.5 V was determined from the voltage transfer curve for the 2-NAND gate to be the voltage at the input switching threshold of the gate.

The measurements on IC B were conducted in a similar manner as that for IC A described above. IC B passed a functional test in which the address decoders were sequenced in low to high order, but failed a ping-pong test. The functional failures occurred when the defective NOR gate outputs were driven high (AB - 00) and then to the high impedance state (AB - 10). These logic failures were verified by observations on the Cambridge DVCS-1500 voltage contrast SEM. Elevation of IDDQ was observed and was consistent with the observations on IC A. The first observed failure condition of occasional high IDDQ following power-up was due to precharge driver and array transistor contention caused by the random occurrence of the precharge state and the latching of certain addresses during power-up.

![SEM picture of a ROM decoder 2-NOR circuit showing an open circuit at the step of the drain line to one of the n-channel transistors.](image-url)

The timing response of the 2-NAND gate (Fig. 3) is shown in Fig. 7(a) when node C was precharged to 0 V. A curve for IDD is not shown on this figure due to inadvertent electrical damage of an input protection diode which prevented the display of the correct IDDQ data. Fig. 7(b) shows the voltage response of the 2-NAND gate when node C was precharged high to 11 V. The voltage responses of the 2-NAND gate to a floating node input are nearly identical to that obtained for IC A even though the structural geometries of the defects are quite different.

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Fig. 7(a). Timing responses of the voltage at node VNAND (Fig. 3) when node C was precharged to 0 V prior to setting node C in a high impedance state at $t = 12$ s.

Fig. 7(b). Node C was precharged to 11 V prior to setting node C in a high impedance state at $t = 12$ s.

III. DISCUSSION

Measurements of the floating node voltage transient response are valuable for the investigation of the memory effect of the stuck-open fault. The time constants measured for the two stuck-open faults reported here were on the order of several seconds, so these stuck-open faults acted as memory faults at typical test and operational clock frequencies. The transient and steady-state properties of stuck-open faults depend on the local physical circuit structure [15,16]. The floating nodes for both types of defects reported here attained a value of approximately 5.5 V, which was near one-half of VDD. Because the 2-NAND input switching threshold was below 5.5 V, the output of the 2-NAND for both IC A and IC B was a weak logic zero value of about 0.4 V. An examination of the area and bias conditions of the p-channel and n-channel transistor drain junctions of the floating node indicated that the floating node voltage was not dominated by drain junction leakage currents. The minimal effect of drain junction leakage on the state of undriven nodes has been observed on other Sandia ICs.

CMOS stuck-open faults are highly significant because they can escape normal functional or stuck-at fault test sets. In the two cases of stuck-open faults described here, a binary up-count sequencing of the ROM decoders did not detect the defect. Two strategies have been used by others for detection of stuck-open defects: (1) use of a stuck-open test set that preconditions each node prior to evaluation by a second test vector [2,3] and (2) use of a stuck-at test set with high node coverage [12,17,18]. Both strategies presently have weaknesses. In the first approach certain CMOS circuit configurations can cause timing glitches in the presence of stuck-open faults [4-11]. These types of subcircuits must first be identified and then corrected in the design since they can lead to erroneous node voltages during the initializing test pattern and subsequent masking of the stuck-open fault. It has also been reported that computer time to generate a stuck-open test set for an 8000 gate circuit was ten times longer than that required for a stuck-at test generation [9]. That particular stuck-open test generator was successful in obtaining 100% stuck-open fault coverage for ICs with 2000 gates or less, but could only attain 70% coverage with a circuit having 8000 gates.

The second strategy for detecting stuck-open faults relies on a high probability of detection of stuck-open faults by stuck-at test sets. One experiment reported that approximately 90% of the stuck-open faults in a sample of 6552 ICs were detected by a 100% stuck-at test set [12]. It was noted in these experiments that the probability of detecting stuck-open faults detection fell as the stuck-at fault coverage fell below 95%. Timco, et al., compared stuck-open and stuck-at fault coverage for an 8-bit CMOS microprocessor by applying 512K test vectors from a weighted pseudo-random binary sequence (PRBS) generator [17]. The stuck-at fault coverage was from 95.5% to 98.4%, depending upon the particular weights applied to the PRBS. In all experiments, the stuck-open fault coverage was about 10% lower than the stuck-at fault coverage. In a different experiment, Timco, et al., reported that an exhaustive test pattern (a binary up-count) detected only 40% of the stuck-open faults in a 4-16 decoder [18]. This evidence suggests that randomness in the stuck-at fault test vector set improves stuck-open fault coverage.

Layout Modification to Reduce Stuck-open Faults

An approach to reducing the probability that stuck-open faults will occur is to implement alternate manufacturing and design techniques. Fabrication processes can be developed to reduce the likelihood of open interconnections due to poor coverage over steps, stress voiding, electromigration, or mask particle defects [19,20]. Another technique to consider is alternate layout styles that replace the drain metal interconnect material with either diffusion or polysilicon material [21,13,22].
intent is to use conducting material that has a lower probability of an open circuit. Koeppe demonstrated a CMOS circuit layout using a ring geometry for the source interconnect diffusion material [21]. This layout typically caused a 2% degradation in propagation delay and had no area overhead. Studies remain to be done for larger circuits that use such layout techniques to reduce stuck-open failure rates. It should be noted that although poor step coverage, stress voiding, and electromigration concerns may possibly be eliminated, open circuits may still occur due to random defects such as particles on masks or in photoresist.

Another layout technique for reducing the probability of stuck-open faults is shown in Fig. 8. This figure shows a conventional layout for a 2-NAND gate in Sandia’s 3 micron, radiation-hardened CMOS technology. The transistor sources are connected to the power supply lines with wider than minimum metal lines. The substrate and p-well contacts at the ends of the metal source lines make contact through a larger contact that simultaneously connects with the diffusion regions and substrate/p-well. The wide metal reduces the probability that an open circuit will occur, and the substrate/p-well ties assure a parallel path from the transistor source regions to VDD/VSS even if opens occur in the metal supply lines. When sources are supplied only through substrate/p-well contacts due to an open circuit in the metalization, some switching time degradation may occur, but unless the failure occurs in a critical path, the increase in propagation delay will be small [21] and the circuit will probably function normally.

Notice also that the transistor drain connections in Fig. 8 use wider than minimum metal. The principle here is to make the transistor interconnect lines as wide as possible without affecting performance and layout area. Too often these lines are minimum width for no good reason. For smaller feature size technologies which do not use guard bands, putting substrate/p-well ties in the sources becomes impractical because they will significantly reduce the effective transistor widths. However, using wide metal for internal connections within a gate usually has no adverse effects on performance or size but reduces the probability of open metal and stuck-open faults.

Stuck-open Fault Detection by IDQQ The measurement of IDQQ is a very sensitive technique for detection of defects in CMOS ICs [23-25,13,14,26]. The time constant of the floating node is therefore important for establishing the validity of the IDQQ measurement technique for the stuck-open defect. Floating nodes cause elevated IDQQ when the final steady state is such that both p- and n-channel transistors are on. If the time constant for this action is small compared to test vector clock periods, the IDQQ in the presence of a stuck-open defects. Fig. 4 showed that IDQQ reached a value of 470 \mu A in the first 200 ms which is normally slow to be detected in the same vector which sets the high-impedance state, but elevated IDQQ may possibly be detected in later vectors.

Figure 8. A layout of a 2-NAND gate that is modified to achieve stuck-open fault avoidance.

It is important to note that the particular failures reported in this paper were always detected by elevated IDQQ measured on a Sentry S20 tester and not always detected by functional testing of the decoder circuit. The results presented here show that elevated IDQQ occurred when stuck-open faults were present in the address decoders of an SRAM IC. This result is significant because of the number of ICs manufactured per year worldwide that contain combinational logic address decoders.

It is also of interest to examine what other circuit configurations might cause elevated IDQQ in the presence of a stuck-open fault. For example, stuck-open faults in control logic for bus-oriented ICs such as microprocessors may cause high IDQQ if the defective logic causes multiple logic blocks to attempt to drive contending data simultaneously onto the data bus. In general, it is possible that stuck-open faults in combinational logic will cause the logic gate inputs to float to voltage levels between the power supply rails and therefore cause high IDQQ.
Stuck-open faults in logic gates that drive precharge circuits may not always cause increased IDDQ. CMOS domino circuit designs employ a precharge state through a single p-channel pull-up transistor. A stuck-open defect in the n-channel logic transistors would not cause a true memory fault since the output node is always precharged to a high state prior to receiving a second set of logic signals [27]. A functional failure would be expected, but IDDQ would not be expected to be elevated in this case.

There are two factors in detection of stuck-open faults by the IDDQ measurement technique. The first is the issue of designs with subcircuits that cause direct contention of transistors when the stuck-open memory state is present. The second factor is that IDDQ elevation due to the floating node took considerably longer than a typical system clock period (Fig. 4). For the defect reported here, IDDQ was 470 uA at 200 ms after the high impedance state was set. If this node was not driven out of the high impedance state during this time, then the fault would be detected. This is of more significance as test times for high reliability VLSI IC's goes well beyond the one second time period of LSI circuits. The IDDQ meter may not guarantee stuck-open fault detection, but it can greatly enhance the probability of detection.

The actual failure frequency for the stuck-open defect is an important issue. Failure frequencies less than 100 PPM for stuck-open faults may not be high enough to justify the test cost. Woodhall, et al., reported an escape rate of 0.1% in their sample of ICs that were evaluated with a 100% stuck-at test set [12]. If the contact misalignment problem in that sample led to some of the stuck-open faults reported, then typical failure rates may be lower. However, the quality of wafer lots varies and each quality measure is not known until after the lot is tested. The limited data available here and in [12] suggest that the stuck-open fault is significant, so tests for these faults and layout designs which reduce their probability should be considered.

IV. CONCLUSION

The measured transient response of stuck-open faults show that this defect acts as a memory fault for normal system and tester clock periods. The data also show that detectable, elevated IDDQ can occur rapidly for some circuit designs. Elevated IDDQ can also occur over many clock cycles as the high impedance node associated with the stuck-open fault undergoes a drift in its voltage. The IDDQ technique is then interpreted as significantly enhancing the detection of stuck-open defects, but not guaranteeing their detection. In view of the reported problems in generating test vector sets which reliably detect stuck-open faults [9, 4-11], an immediate recommendation is to redesign cell layouts for stuck-open fault avoidance.

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