AM/PM Nonlinearities in SiGe HBTs

Stephen Horst and John D. Cressler
School of Electrical and Computer Engineering
777 Atlantic Drive, N.W., Georgia Institute of Technology
Atlanta, Georgia 30332–0250 USA
E-mail: shorst@ece.gatech.edu

Abstract—An analysis of AM/PM nonlinear distortion in advanced SiGe HBTs is presented. The results show that an optimum bias point exists in the high-injection collector current density regime as the device nears BVCEO. At this point, the phase deviation remains close to zero, even as the transistor gain goes into compression. This effect can be further optimized by matching the output of the device to its optimum OIP3 impedance. These results should prove useful for power amplifier design for high data rate electronic systems, which typically require high peak-to-average power ratios.

I. INTRODUCTION

Linearity often plays a limiting role in high dynamic range RF circuits using silicon-based semiconductor devices. Research efforts to improve linearity in Silicon Germanium (SiGe) devices and circuits have typically focused on gain compression or intermodulation distortion; metrics that use a change in input amplitude to reveal changes in the output amplitude characteristics, or AM/AM nonlinearities [1]. An important parameter often overlooked in many applications is the phase deviation at large signal, so-called AM/PM nonlinearities. The concept of AM/PM distortion is not new, and first appeared in the development of communication systems theory [2], [3]. Recently, AM/PM nonlinearities have been analyzed in integrated varactor diodes used in resonant tanks to determine its effect on phase noise in oscillators [4]. A model to predict AM/PM distortion in HBTs using Volterra series was also recently presented [5], although to our knowledge no measured data was ever given to support their theory.

AM/PM distortion manifests itself as a change in phase with respect to the input power applied to the device. In an ideal linear system, the frequency domain phase response would remain constant across input power. A nonlinear signal, however, will introduce phase changes in the fundamental frequency similar to the spurious harmonics also generated. This is often overlooked because it is a critical concern only in certain types of electronic systems. The phase changes introduced as the device compresses are typically on the order of a few degrees, but even this small shift can have a significant impact on the operation of high data rate systems such as wireless LAN (WLAN). In the case of WLAN, the binary decision boundaries to interpret the 64 QAM constellation require very accurate amplitude and phase information be preserved in order to avoid bit error rate degradation. A phase error introduced by AM/PM distortion can lead to a significant increase in error vector magnitude (EVM), and in turn, bit error rate, degrading overall system performance. A similar situation exists for large phased arrays that use attenuation for sidelobe shaping. The elements operating at full power are potentially in greater compression than their attenuated counterparts and if so will exhibit a different phase shift relative to them. This undesired deviation leads to errors in the array’s radiation pattern. To the best of our knowledge, no measurement data exists on the AM/PM characteristics of an advanced SiGe technology, often employed in wireless applications where such issues could potentially arise, and is presented here for the first time.

II. MEASUREMENT SETUP

In order to observe the nonlinear phase deviation across all of the desired parameters, an integrated load-pull setup was used, which allowed for consistent calibrated measurements across various conditions. Shown in Figure 1, this Focus Microwaves system uses custom-built high-impedance probe tuners to tune the load to gammas of up to 0.88. Once calibrated, a suite of measurements, including S-parameters, output power, gain compression, and third-order intercept point can be taken without ever lifting the microwave probes. A static measurement was used to characterize the AM/PM conversion, as outlined in [6]. This technique uses a network analyzer configured for gain compression measurements. Since AM/PM conversion is a phenomena that appears in the device during weakly nonlinear operation, it must be in compression to observe the effect. By measuring the change in phase of the calibrated insertion loss measurement as the device is
driven into compression, the nonlinear phase deviation can be observed. An ideal device with no AM/PM conversion would show a flat phase response across input powers.

The test was conducted on a commercial 130 nm SiGe BiCMOS technology platform. This is IBM’s third-generation, high-performance production technology featuring an $f_T$ of 200 GHz and $f_{MAX}$ of 285 GHz as seen in Figure 2. A 0.12x18 μm SiGe HBT was measured, because it is the largest emitter size supported by the design kit and is a good representation of a geometry that could be found in a typical power amplifier design. A measurement frequency of 10 GHz was chosen because of load tuner limitations, but this approach can be easily extended into WLAN bands, as needed.

### III. AM/PM ACROSS BIAS

#### A. Bias Mode

An initial test was run to get a feel for the overall nonlinear phase performance of the SiGe HBT. Using the measurement setup described, the device was biased using both a voltage source and a current source on the base-emitter junction. An equivalent simulation was run using GoldenGate, with the design kit provided VIBIC SiGe HBT model. The results are shown in Figure 3 as phase deviation across gain compression. Recall that an ideal response should give zero phase deviation for any power level. Plotting this phase deviation over gain compression rather than the absolute power level is intended to give insight into phase distortion with respect to more familiar amplitude distortion metrics. In the current driven case in Figure 3, this implies that at a gain compression of 1 dB, when the input power is set to the $P_{dd}$ point, the phase will shift by slightly more than two degrees.

Figure 3 indicates that the VIBIC model is reasonably accurate at predicting the phase deviation when the transistor is current biased, but not so accurate when a voltage bias is applied. We hypothesize that although the SiGe HBT is modeled as a transconductance device for AC signals, where small variations on the input voltage correlate with a change in the output current, DC bias is defined by the fixed parameter current gain, $\beta$. Thus, when a current is used to bias the base, the DC bias point is well-defined, since there is a fixed reference for $\beta$. This situation is similar to the common current mirror configuration used to bias many integrated circuits. On the other hand, when a voltage bias is instead applied to both the base-emitter and the collector-emitter junction, there is no fixed reference for $\beta$, and the DC bias point tends to float slightly. While this is still a valid mode of operation, the large-signal S-parameter simulation uses a fixed DC bias point across the entire power sweep, leading to the discrepancy shown in Figure 3. Note that a current bias cannot be used on the output terminal for a simple common-emitter test structure because that would leave $V_{CE}$ floating, and changes on the input voltage would lead to output voltage changes that would cause the transistor to go constantly in and out of saturation.

In fact, using an active voltage bias may potentially represent a way to mitigate AM/PM distortion, as the measured data shows almost no phase deviation, well into gain compression. However, this would require knowledge of how to best capture a floating bias point in an RF simulation, and is presently still being researched. The remainder of the data presented here uses current bias conditions.

#### B. Bias Point

AM/PM conversion was examined for several bias points across the forward active region of the device. Three different current bias states were tested with $V_{CE}$ set to 1.0 V, about mid-range between saturation and the $BV_{CEO}$ of the HBT. Shown in Figure 4, the low-injection condition corresponds to a collector current density of about 1.0 mAm$^{-2}$, while the mid-range and high-injection conditions correspond to 3.2 mAm$^{-2}$ and 10.0 mAm$^{-2}$, respectively. The results demonstrate that as the device moves toward peak-$f_T$ bias, not only does the gain compression decrease, as is evident by the shorter range on the x-axis, but the phase deviation actually flattens as the device goes into the early stages of compression. This 0-2 dB gain compression region is important because beyond that, traditional AM/AM nonlinearities such as third-order intercept and gain compression itself will begin to dominate the bit error rate.

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**Fig. 2.** Maximum oscillation frequency, $f_{MAX}$, and unity gain frequency, $f_T$, for a 0.12x18 μm IBM 8HP SiGe HBT. The marked locations on the $f_T$ plot show the bias points tested in this study.

**Fig. 3.** AM/PM conversion with forced voltage and current bias on the base. The solid line represents measurements, while the dashed line is a GoldenGate simulation based on a calibrated VIBIC model.
Using the information provided by Figure 4, we next biased the device at the high-injection current density state and swept $V_{CE}$ across three different voltages. This time 0.5 V, 1.0 V, and 1.5 V were used to bias the device near saturation, mid-range, and near breakdown, respectively, as shown in Figure 5. The measured results indicate that although the phase deviation rises sharply after 2 dB of gain compression, biasing the device near breakdown effectively mitigates AM/PM distortion below that compression, which can be a very useful buffer zone to take advantage of in circuit design.

Using our optimal bias point of high-injection at near avalanche breakdown ($BV_{CEO}$), we then turned to simulations to observe how well the SiGe HBT VBIC model captures AM/PM distortion under this condition. The results in Figure 6 show that for the region of primary interest, from 0-2 dB gain compression, the simulation accurately models the data. This is good news for power amplifier design, since biasing in this region will give the largest output power. One cannot, however, overlook the implications for the rest of the transceiver chain due to AM/PM distortion. Low noise amplifiers, in particular, are often biased at low injection and can easily have a strong input signal send them into compression, thereby accentuating AM/PM distortion.

**IV. AM/PM ACROSS LOAD**

Since measurements across bias indicate that AM/PM conversion will have the least affect on devices biased for high output power, a logical follow-up question is whether a power match will enhance or degrade this effect. To test this, a load-pull measurement was run across various linearity parameters. The tuners were then set to these values, the switches were toggled to the network analyzer, and static phase deviation measurements across input power were taken, similar to the previous procedure. The results in Figure 7 show that a match to maximum output power similar to the procedure used to design power amplifiers in fact degrades the nonlinear phase deviation with respect to the 50Ω measurement.

Since matching to the maximum output power impedance degrades the AM/PM response, the next step is to determine what impedance provides the optimal match to minimize AM/PM conversion. We know that the effect derives from the nonlinear response of the device as the input power moves...
from small-signal to large-signal. Therefore, since we have no way of directly measuring the phase during the load-pull measurement, it makes sense to associate low AM/PM conversion with a corresponding AM/AM measurement. In this case, we chose to maximize the third order intercept point ($IP_3$). As seen in Figure 7, a match to this impedance does in fact improve the AM/PM distortion by further flattening the distortion response to nearly zero degrees well into gain compression. The $OIP_3$ contours from the load pull measurement can be observed in Figure 8. The optimal match, which gives an $OIP_3$ of 16.9 dBm, is very close to 50 Ω. As a reference, the impedance for the maximum output power is also plotted in Figure 8.

Based on devices measured from several different wafer lots, we theorize that the flattening effect initially observed at 50 Ω is merely a byproduct of its proximity to the optimum linearity load point. Over a sample size of two transistors across three different wafer lots, devices whose maximum $OIP_3$ load point was closer to 50 Ω generally showed improved phase flatness at 50 Ω. AM/PM distortion at the optimum $OIP_3$ load deviated less than 1 degree from small signal at gain compressions of less than 2 dB for all samples. These observations seem to indicate that an optimum matching condition exists for AM/PM distortion that is closely tied to maximizing $OIP_3$. Since this load impedance differs from the maximum output power impedance typically used to design power amplifiers, a trade-off between linearity and output power seems applicable similar to the noise figure and gain power amplifiers, a trade-off between linearity and output power. OIP maximizes maximum output power impedance typically used to design

Future work on this topic would involve constructing a mathematical model to explain the behavior seen in this experiment, analyzing the differences between common emitter, collector, and base configurations, as well as devising a means to measure AM/PM conversion during load-pull rather than trying to infer performance from related AM/AM metrics.

VI. ACKNOWLEDGEMENT

This work was supported by NASA. The authors are grateful to L. Kuo, T. Thrivikraman, and the members of the SiGe team at Georgia Tech.

REFERENCES