A 40% PAE Linear CMOS Power Amplifier with Feedback Bias Technique for WCDMA Applications

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Abstract — A highly efficient CMOS linear power amplifier for WCDMA applications with feedback bias technique is presented. The method involves connecting the gates of common-gate devices of the driver stage and the power stage in cascode configurations by a feedback network for enhancing linearity. To achieve high efficiency and linearity simultaneously, large-signal IMD minimum (IMD sweet spot) is properly used at the desired output power level. The proposed PA was fabricated in a 0.18-μm CMOS technology. The experimental results demonstrate a gain of 26 dB, a maximum output power of 26 dBm with 46.4% of peak PAE, and a linear output power of 23.5 dBm with 40% PAE using a 3GPP WCDMA modulated signal. Both simulation and measurement results show an excellent large-signal IMD minimum at the output power using a WCDMA modulated signal.

Index Terms — bias, CMOS, efficiency, feedback, linearity, power amplifier, sweet spot, WCDMA

I. INTRODUCTION

Recent progress of CMOS technology is remarkable, and it makes possible the potentials of a fully integrated RF front-end system. However, the power amplifier (PA) is still a bottleneck for the complete integration because of CMOS technology's inherent characteristics such as low trans-conductance, low reliability, and large parasitic elements.

Because of the low transconductance of CMOS technology, multi-stage cascade methods or larger power cells are required to generate the same output power and gain compared with other III-V compound technologies. However, this creates larger parasitic elements within the PA, and can be the cause of the low efficiency and linearity.

For the reliability of devices, a cascode configuration with a thick-oxide transistor is generally used to prevent oxide breakdown by large voltage swings, or hot carrier degradation which can increase the threshold voltage so that it degrades the performance of the device [1]. However, in the cascode configuration, there might be an additional non-linearity from the common-gate (CG) device compared to the common-source (CS) amplifier topology. The feedback bias technique can improve the PAs’ linearity by reducing non-linearity effects that can occur in the CG device of the cascode structure.

The proposed CMOS linear PA is designed with a two-stage and single-ended cascode configuration which incorporates a feedback bias technique to overcome those CMOS technology’s drawbacks. Also, to achieve high efficiency and good linearity, large-signal IMD minimum (IMD sweet spot) is properly used. [2]

The CMOS linear PA is designed for WCDMA application and the required specifications are satisfied. The design specifications for WCDMA PAs are listed in Table I [3].

<table>
<thead>
<tr>
<th>Specifications</th>
<th>1.92GHz - 1.98GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>(Band I)</td>
</tr>
<tr>
<td>Maximum Output Power</td>
<td>(Power class 3)</td>
</tr>
<tr>
<td>ACLR (3.84MHz main channel)</td>
<td>-33dBc @ 5MHz offset</td>
</tr>
<tr>
<td></td>
<td>-43dBc @ 10MHz offset</td>
</tr>
</tbody>
</table>

II. CIRCUIT DESIGN METHODOLOGY

In linear PA design, high efficiency and good linearity are the most important parameters. As generally known, class A has high linearity with low efficiency, while class B and C have higher efficiency with degraded linearity compared to class A. Since efficiency and linearity are in trade-off relationship, class AB can be the best option considering both of them [4].
Considering PA operation, the large-signal analysis is more applicable for linearity IMD analysis than small-signal analysis. As the input power increases, higher-order terms of Volterra series expansion become dominant, and the combination with the compressing non-linearity of the saturation-to-linear region transition can result in the IMD sweet spot that occurs close to compression output power level [2]. In this PA design, deep-class AB is employed and the bias voltages are set to have the IMD sweet spot appearing near the compression point. By carefully optimizing a bias point at near threshold, which is a deep-Class AB operation, it is possible to adjust the relative position of the sweet spot and making it possible to achieve good linearity with high efficiency by placing the sweet spot at the desired output power. Based on simulation experiences, under the -25 dBc two-tone IMD3 in harmonic balance simulation was aimed instead of the -33 dBc ACLR for 3GPP WCDMA PA linearity specification in time-consuming envelope simulations.

Fig. 1 shows a simplified schematic of the suggested two-stage single-ended CMOS linear PA. A single-ended topology is chosen for easier integration, cost-effectiveness, and avoidance of baluns although a differential configuration has the advantage of the even harmonics control. [5] To reduce the noise coupling with other components on the same silicon substrate, a deep N-well [6] is employed for both the driver and power cells. For the reliability of the devices at 3.4V operation, a 0.4-um thick-oxide NMOS transistor is used in the power stage cascode CG transistor, and 0.18-um NMOS transistors are used for the both of CG and CS in the driver stage to compensate for the low RF power gain of the thick-oxide CG transistor in the power stage.

III. FEEDBACK BIAS TECHNIQUE

In PA design, parasitic capacitances are unavoidable and exist between the ports of a transistor. In the proposed PA, a feedback bias technique, which connects the gate of the common-gate transistor in the power stage, \( G_2 \), and the gate of the common-gate transistor in the driver stage, \( G_1 \), by a feedback network, is adopted to enhance linearity using the leakage signals through the parasitic capacitances of the CG-transistor in Fig. 1.

Although the gate of the common-gate device is ideally AC grounded in a cascode topology, there exist signals that are coupled from the both drain and source by gate-source capacitance, \( C_{gs} \), and gate-drain capacitance, \( C_{gd} \) respectively. They exist for both the driver and power stage cascode amplifiers. By connecting \( G_1 \) and \( G_2 \) with the carefully optimized feedback network, the gate leakage signal of \( G_2 \) is fed back to \( G_1 \) with 180 degree phase shift created by feedback network. Therefore, the signal fed back from \( G_2 \) to \( G_1 \) is in-phase with the source and drain waveforms, which means that the variation of the CG device’s operation is minimized because the voltages between the ports are maintained. It can reduce the additional non-linearity effects that can occur by variations of parasitic capacitances in the CG device within a cascode topology. Fig. 2 shows the waveforms with feedback bias and the waveforms without feedback bias. Because of the large voltage swing, the operation region of
the CG transistor continuously changes saturation region, triode region, and cutoff region. With this feedback bias technique, the ratio of the cutoff region of CG transistor is reduced and triode region is also reduced during the turn-on region. By using the technique, the variation of the operation region of CG transistor is minimized, so that it improves the linearity of the proposed PA. However, as the voltage of G1 follows the source voltage of CG in both positive and negative swings near the DC value of G1, a non-optimal gain can be achieved compared to the conventional cascode PA which has RF ground at gate node of CG transistor.

The feedback network is a T-network, which consists of an inductor and two capacitors. The inductor is implemented as a bonding wire inductance to ground and the capacitors in the feedback network also act as AC ground for the cascode topology. Thus, there are no additionally required components for the feedback bias technique since the capacitors and bonding wire inductor of the feedback network are essential components to the cascode amplifier topology. Also, the feedback bias technique does not use the signal path of the PA, so that it can improve linearity without affecting operation of the PA.

IV. EXPERIMENTAL RESULTS

Fig. 3 shows a photograph of the fabricated CMOS PA, which has 1.6 mm x 0.52 mm chip area. All components are fully integrated to one chip. To verify the chip, an FR-4 PCB evaluation board is used and the chip is mounted on the ground plate of the evaluation board. By connecting multiple bonding wires to the ground, it can minimize source degeneration effects of both driver and power cells which typically can lead to the decrease of gain.

![Photograph of the feedback CMOS power amplifier.](image)

Fig. 4 shows the comparison of simulated and measured Power Added Efficiency (PAE) and gain of the proposed amplifier. From the graph, maximum output power is reduced from 27.5 dBm to 26 dBm and peak efficiency also decreased from 55.4% to 46.4%. The 1-dB gain compression point is 25.4 dBm. The measured output power with a linear 3GPP WCDMA modulated signal is 23.5 dBm with 40% PAE and the DC current consumptions of the driver and power amplifier were 27mA and 143 mA, respectively.

Fig. 5 shows the measured IMD3 and ACLR results. A two-tone test is performed at 1.95 GHz center frequency with 5 MHz tone-spacing. From the measurement results, under the -25dBc two-tone IMD3 guarantees the required linearity ACLR of -33 dBc. Also, the sweet spot appears at the desired output power of 22dBm to achieve lower IMD3.

Comparisons are made between the PA with the feedback bias and the PA without the feedback bias in Fig. 6. The measurement results compare the ACLR performance. As shown in the Fig.6, the feedback bias technique improved ACLR at the desired high power regime having much margin of ACLR. The linear output power is significantly increased from 22.7 dBm to 23.5 dBm using a 3GPP WCDMA modulated signal because of the increase of the ACLR margin.
V. CONCLUSION

In this paper, the highly efficient CMOS linear PA is demonstrated for WCDMA application. The proposed feedback-biased PA was fabricated in a 0.18-um standard CMOS technology and to achieve high efficiency and good linearity, IMD sweet spot is properly used at the desired output power. The feedback bias technique, which incorporates the gate of common-gate transistors of the driver stage and the power stage in cascode configurations, is used for improving linearity of the common-gate transistor, which is verified in the measurement results. Experimental results demonstrate the power gain of 26 dB, and a max output power of 26 dBm with 46.4% peak PAE and a linear output power of 23.5 dBm with 40% of PAE using a 3GPP WCDMA modulated signal.

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REFERENCES


