Total Dose Testing of 10-Bit Low Voltage Differential Signal (LVDS) Serializer and Deserializer

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Abstract—Commercial deep submicron (< 0.25 micron) CMOS technology exhibits excellent total dose hardness. National Semiconductor LVDS serializer and deserializer circuits, manufactured in this process, were tested to over 115 krd(Si) and 65 krd(Si) respectfully, without failure. Testing proved to challenge traditional test techniques, as these parts ran at parallel data rates up to 40 MHz.

I. INTRODUCTION

The total dose response of National Semiconductor DS92LV1021 serializer and DS92LV1212 deserializer chips [1] was evaluated. To provide for high-speed (40MHz), in-situ characterization of these parts, an HP82000 tester was sited within 10 meters of the Cobalt 60 irradiator.

The evaluation consisted of 1) test software creation, 2) design and manufacture of test fixtures with extended I/O cables, 3) system debug with extended I/O cables attached and 4) radiation exposure, data collection and analysis.

The National Semiconductor DS92LV 102 1 serializer and DS92LV1212 deserializer chips are fabricated using 0.25~CMOS-8 processes. A recessed oxide (bird's beak) isolation was used, which appears harder than National's shallow trench isolation.

LVDS (low voltage differential signal) is a widely used standard protocol for high-speed serial data transmission [2]. For example, on most laptop computers it is used to link the liquid crystal display to the computer/keyboard unit. The National Semiconductor DS92LV1021 serializer chip samples a 10-bit parallel CMOS/TTL data bus at rates from 16 to 40 million samples per second (MSPS) and converts this data to serial format. The serial data is then transmitted, at a rate of 160-400 Mbps, over a heavily loaded differential back plane or unshielded twisted pair cable at distances up to 10 meters, utilizing the standard LVDS protocol [2]. The DS92LV1212 deserializer chip accepts this serial input and reconverts it to 10-bit parallel data. Clock-to-data and data-to-data skew is eliminated since the clock is recovered from the serial data stream. Synchronization is achieved with an internal phase-lock loop (PLL) incorporated in the deserializer chip. This PLL requires approximately 1024 cycles (51.2 μs @ a 20 MHz clock rate) to establish lock, which is indicated by the assertion of the LOCK bit on the deserializer chip. This parameter is referred to as PLL lock time and varies from 35 μs to 60 μs @ 20 MHz and 20 μs to 30 μs @ 40 MHz during normal operation, depending upon configuration.

II. TEST SETUP

The two device types were tested as a pair, with one device being irradiated in the gamma source and the other used to receive data back at the HP82000 tester. The two chips provided the serial link and the parallel I/O pins were addressed by the tester (fig. 1). All tests were performed with a nominal Vcc of 3.4 V.

Figure 1. System Block Diagram

Four electrical test routines were developed, and run sequentially during active irradiation: 1) word error count, 2) PLL lock time, 3) dynamic current and 4) static current. The word error count measures the number of transmission errors observed during the execution of a 100k-word, pseudo-random numeric (PRN) generated vector set. It is defined as a word error because the tester counts single or multiple bit errors in a 10-bit data word as a single error. When a single bit error is observed in the 10-bit word, the word error count is equivalent to a serial bit error rate (BER) commonly measured in serial data links [3]. With 100,000, 10 bit words in the vector set, an effective serial data pattern of 1Mbits (or
Figure 2, Serializer. A serializer s/n3 was tested using a parallel data rate of 20MHz. The chip remains functional until word error count hits full scale at 169 krd(Si). This graph illustrates the real-time data acquisition capabilities of the HP82000 test system.

PLL Lock time is the time required for the deserializer to set its LOCK bit after the serializer initiates a SYNC pattern. In sync/lock mode, the serializer transmits a standard SYNC pattern until a LOCK signal is received from the deserializer, at which time normal data transmission commences. For the PLL lock time test, the sync/lock mode of operation was used exclusively. The random lock mode (locks on normal data stream), takes much longer (up to milliseconds), is bit pattern dependent and can establish a false lock with certain data patterns, and was not used in as part of our tests. Dynamic current was measured during normal operation at the test clock speed, while static current was measured when the powerdown signal was applied, with no clocks. The deserializer dynamic currents were higher than nominal due to an anomaly in the test fixture, as will be discussed in the results section.

A custom test fixture was developed such that either chip could be placed in the radiation source independently, allowing active in-situ testing. The maximum 10 meter cable length was used between the LVDS driver and receiver, to provide worst case loading. Test data was displayed “real-time” during in-situ testing with an update rate of 0.5 Hz, as shown in figure 2.

Several key features of the HP82000 tester were utilized for this test, including: sequencer programming within a vector set, large (100k) PRN vector data sets for digital input data, word and bit masks, error counting features, and long propagation delays of several clock cycles between data clocked into the serializer and data out of the deserializer. Figures 2 and 3 demonstrate the graphing abilities of the HP82000 semiconductor test system and VEE Pro software. The ability to visualize data in real-time as the test was proceeding provide increased confidence in data integrity and expedite the testing/analysis process.

Custom serializer and deserializer circuit boards, incorporating a 28L SSOP device under test (DUT) sockets, were manufactured. This socket was required to facilitate radiation testing for groups of IC chips by enabling quick insertion/removal of the DUT. The design was based on National Semiconductor’s evaluation boards with a minor design change eliminating an inverter, which would have been susceptible to radiation damage. The HP82000 tester easily emulated the function of this inverter.

III. RESULTS

Six DS92LV1021, LVDS serializer and seven DS92LV1212 LVDS deserializer IC’s were total dose tested during February and March of 2001. A Shepherd Model 484 Cobalt 60 source was used at a dose rate of 15 rd/s. The test circuit was placed in a Pb/Al container to minimize dose enhancement effects, with all I/O cables running 10 meters to the HP82000 semiconductor tester. All measurements were
Table 1. Total dose test summary for DS92LV1021 LVDS serializers (Tx) and LVDS DS92LV1212 LVDS deserializers (Rx). Sample rate refers to the data acquisition rate and was typically set to one measurement cycle per 2 seconds during exposure (a single measurement cycle takes ~1.6s).

<table>
<thead>
<tr>
<th>Type</th>
<th>S/ n</th>
<th>Parallel Data Rate</th>
<th>Pre-rad Sample Rate</th>
<th>Sample Rate During Irradiation</th>
<th>Post-rad Sample Rate</th>
<th>Word Error Failure Level [krad(Si)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx</td>
<td>1</td>
<td>20 MHz</td>
<td>0.5 Hz</td>
<td>0.5 Hz</td>
<td>15 min/point</td>
<td>150</td>
</tr>
<tr>
<td>Tx</td>
<td>2</td>
<td>20 MHz</td>
<td>(1) 0.5 Hz</td>
<td>0.5 Hz</td>
<td>15 min/point</td>
<td>168</td>
</tr>
<tr>
<td>Tx</td>
<td>3</td>
<td>20 MHz</td>
<td>0.5 Hz</td>
<td>0.5 Hz</td>
<td>15 min/point</td>
<td>169</td>
</tr>
<tr>
<td>Tx</td>
<td>4</td>
<td>20 MHz</td>
<td>0.5 Hz</td>
<td>(2) 10 min/point</td>
<td>15 min/point</td>
<td>117</td>
</tr>
<tr>
<td>Tx</td>
<td>5</td>
<td>40 MHz</td>
<td>0.5 Hz</td>
<td>0.5 Hz</td>
<td>15 min/point</td>
<td>146</td>
</tr>
<tr>
<td>Tx</td>
<td>6</td>
<td>40 MHz</td>
<td>0.5 Hz</td>
<td>0.5 Hz</td>
<td>15 min/point</td>
<td>135</td>
</tr>
<tr>
<td>Tx</td>
<td>7</td>
<td>40 MHz</td>
<td>(3) 15 min/point</td>
<td></td>
<td></td>
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</tr>
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<td>Rx</td>
<td>8</td>
<td>20 MHz</td>
<td>0.33 Hz</td>
<td>0.33 Hz</td>
<td>15 min/point</td>
<td>92</td>
</tr>
<tr>
<td>Rx</td>
<td>9</td>
<td>20 MHz</td>
<td>(1) 0.33 Hz</td>
<td>0.33 Hz</td>
<td>15 min/point</td>
<td>79</td>
</tr>
<tr>
<td>Rx</td>
<td>10</td>
<td>20 MHz</td>
<td>0.33 Hz</td>
<td>0.33 Hz</td>
<td>15 min/point</td>
<td>65</td>
</tr>
<tr>
<td>Rx</td>
<td>11</td>
<td>20 MHz</td>
<td>(2) 10 min/point</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rx</td>
<td>12</td>
<td>38.46 MHz</td>
<td>0.33 Hz</td>
<td>0.33 Hz</td>
<td>15 min/point</td>
<td>72</td>
</tr>
<tr>
<td>Rx</td>
<td>13</td>
<td>38.46 MHz</td>
<td>0.33 Hz</td>
<td>0.33 Hz</td>
<td>15 min/point</td>
<td>114</td>
</tr>
<tr>
<td>Rx</td>
<td>14</td>
<td>38.46 MHz</td>
<td>(3) 1 min/point</td>
<td>(4) 0.5 Hz</td>
<td>15 min/point</td>
<td>106</td>
</tr>
</tbody>
</table>

(1) Extended pre-rad to establish normal operating values at 20MHz.
(2) Data was taken every 10 minutes, the remainder of the cycle the part was biased with the PWRDN (static mode) signal applied.
(3) Extended pre-rad to establish normal operating values at 38.46MHz and 40MHz.
(4) Temperature was periodically measured during these tests.
(5) Word error count exceeds 100 counts per 100k, 10bit words (1M bits) for any given test cycle.
(6) Control sample (not irradiated).

It should be noted that the "Word Error Failure Level" is defined as the first dose where word error rate exceeds a count of 100. By the time word count exceeded 100, both static and dynamic currents had degraded significantly, and the PLL lock time had degraded as well. Current and lock time degradations may be more important to some applications than the word error level. Figure 2 shows results for serializer/s 3. The dynamic and static currents steadily made "in-situ", enabling data analysis to begin in real-time. Table 1 summarizes the parts tested.

**Figure 3, Deserializer.** This graph shows the response of deserializer s/n 8. Note the steady increase in word errors while the PLL lock time remains constant to over 100 krad(Si). The large drop in dynamic current at 120 krad(Si) is because when the deserializer losses LOCK, its outputs go TRI-STATE.
increased with irradiation, while the PLL lock time abruptly jumped, first at about 93 krd(Si) but the serializer remained functional, with no observed word errors, up to a total dose of 169 krd(Si). This is a typical device response with the standby current drifting above the rated specification of 5 mA, while dynamic current remained below the 55 mA specification.

For the purposes of this paper, “functional” means data transmission is still possible with a word error count less than 100 out of the 100,000 vectors (0.1%). Failure level in table 1 refers to the total dose level where data transmission is starting to be compromised based on a word error count exceeding 100. In the case of the serializer, this happened very abruptly. For example, in figure 2 the word error count remained at zero until it momentarily went full scale at 169 krd(Si), recovered and again went full scale at 179 krd(Si), this time without recovery. It this case 169 krd(Si) is reported as the failure level.

Figure 3 shows the response of deserializer s/n8 operating at a 20 MHz parallel data rate. As with the serializer, the Idd (DUT Vcc current) currents show substantial increases. This is particularly dramatic for the static Idd current which goes from a pre-rad level of 6 uA to near 50 mA at device failure level of 92 krd(Si).

The dynamic Idd currents for all deserializer data is higher than the listed specifications of 40 mA (@16 MHz). After testing was completed, it was discovered that current limiting resistors for the deserializer digital drive lines were installed at the tester end of the 10 meter cable, but should have been at the DUT end. This introduced a highly capacitive load, which nearly doubled the dynamic current. This problem was not noted at the time of test because a preliminary National Semiconductor data sheet had “to be decided” (TBD) for the maximum limits of dynamic and static current, or 80 mA and 10 uA for the typical levels. Because the typical current was listed as 80 mA, our observed 90 mA dynamic current did not seem out of line. This can be easily correct for future tests. The impressive fact is that the deserializer outputs drove this heavy load at its rated 40 MHz rate. Unfortunately, the load may have impacted the observed failure points. While it seems likely that the results would be better had we moved these resistors, this is only speculation on our part.

It was also observed that at total doses of less than 200krd(Si), many of the failed devices would once again become operational after a short room temperature anneal. Figure 4 shows a complete test cycle composed of pre-rad, rad and post-rad (anneal) data of the DS92LV1021 serializer, s/n 3. The data depicts a strong correlation between word error rate and lock time. This indicates a possible failure in the SYNC/Lock section of the serializer. Further investigation on the failure mechanism is needed.

It can also be observed that anneal for the currents and PLL lock time quickly levels off. Post-rad data was taken for up to
five days with little change beyond this initial recovery. A more detailed study of the anneal characteristics could be interesting.

The deserializer exhibited almost identical anneal characteristics with the same correlation between word error rate and lock time as seen in figure 4.

Subtle differences were observed between the various in-situ test configurations. The most dramatic among the serializers tested was the lower failure level observed for s/n4 (table 1). This part was biased in standby mode with no clocks applied (static). The test cycle (1.6 sec) was run once every 10 minutes. Upon completion, standby mode was again applied. The parts running at a parallel data rate of 20 MHz performed slightly better than those running at 40 MHz.

Another observation among the 40 MHz serializer data was the word error count went full scale with no noticeable change in the PLL lock time. This phenomena only occurred in the serializers running at 40 MHz. In all other cases there was a correlation between the PLL lock time and word error count.

The deserializers were more stable running at a parallel data rate of 38.46 MHz, rather than 40 MHz (most likely related to the loading problem discussed above).

Of note among the various deserializer configurations was at 20 MHz (fig. 3) the word error count exhibited a gradual increase. In all cases other than 20 MHz deserializers the word error count abruptly went full scale similar to the behavior observed in figure 2.

IV. CONCLUSIONS

The National Semiconductor DS92LV1021 and DS92LV1212 circuitry is very forgiving and remains operational even after substantial parametric shifts. DS92LV1021's remained functional well over 115 krd(Si), however there were substantial increases in the static current, dynamic current and system lock time prior to functional failure. The system lock time more than doubled, going from 50 µs to 125 µs at 100 krd(Si) in the case of s/n 3. This could be the result of a shift in the synchronization pattern circuitry, which is generated by the serializer in order to lock the clocks. System designers should take the effects of timing and current shifts on system performance under consideration.

Post-rad annealing at room temperature showed modest recovery of the parametric shifts, and total recovery of functionality within a couple of hours.

The lowest failure observed for the DS92LV1212 was 65 krd(Si), while some parts remained operating above 100 krd(Si). However, with proper digital data driver line loading, it is possible that failure levels could have been higher. The power down current degradation for this part was extreme, with a pre-rad level of 6 uA increasing to over 3 mA at 50 krd(Si) and near 40 mA at 100 krd(Si). Very little pre/post radiation shift was observed in lock time, indicating that the PLL remains stable at these radiation levels.

V. REFERENCES

[1] Data Sheets, National Semiconductor Corporation, (800)772-9959