ENHANCED PERFORMANCE OF CdS/CdTe THIN-FILM DEVICES THROUGH TEMPERATURE PROFILING TECHNIQUES APPLIED TO CLOSE-SPACED SUBLIMATION DEPOSITION

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ABSTRACT

We describe a methodology developed and applied to the close-spaced sublimation technique for thin-film CdTe deposition. The developed temperature profiles consisted of three discrete temperature segments, which we called the nucleation, plugging, and annealing temperatures. We have demonstrated that these temperature profiles can be used to grow large-grain material, plug pinholes, and improve CdS/CdTe photovoltaic device performance by about 15%. The improved material and device properties have been obtained while maintaining deposition temperatures compatible with commercially available substrates. This temperature profiling technique can be easily applied to a manufacturing environment by adjusting the temperature as a function of substrate position instead of time.

INTRODUCTION

Thin-film CdS/CdTe solar cells are strong contenders for large-scale terrestrial photovoltaics, with devices and modules realizing improved efficiencies during recent years. One of the most promising techniques used to deposit thin-film CdTe is close-spaced sublimation (CSS). The CSS technique has demonstrated success in both the laboratory and manufacturing environments [1,2].

In this study, we describe a methodology that we have developed and applied to the CSS technique for thin-film CdTe deposition. By modifying and optimizing the source and substrate temperature profiles during deposition, we have significantly improved both the material properties of CdTe thin films and the performance of CdS/CdTe photovoltaic devices fabricated from these films. The influences of deposition temperature profiles on grain growth, film quality, and device performance are assessed using scanning electron microscopy (SEM), atomic force microscopy (AFM), current-voltage (I-V) measurements, and spectral response (QE) analysis.

EXPERIMENTAL

The CSS technique has been used by many groups to grow single-crystal materials as well as polycrystalline thin films [3-6]. In our CSS apparatus, the source and substrate susceptors were independently heated by quartz lamps whose output was controlled by programmable temperature controllers. The space between the source and substrate susceptors was 2 mm and was maintained using quartz spacers. The entire assembly was enclosed in a quartz tube with gas inlet and exhaust.

Temperature profiles are defined by separately controlling the source and substrate temperatures as a function of deposition time. This process can be translated to a manufacturing environment by adjusting the temperature as a function of substrate position. In this study, the source and substrate temperatures were controlled within the range of 65°C-68°C and 500°C-645°C, respectively. Total system pressure ranged from 10-30 Torr and was measured with a capacitance manometer pressure transducer.

The CdS/CdTe photovoltaic device configuration used in this research work consisted of Glass/SnO2/CdS/CdTe/HgTe/Graphite and silver paste structure [7]. About 4 to 6-μm-thick CdTe films were deposited onto the Glass/SnO2/CdS substrates by the CSS technique with a deposition rate of about 1 μm/min.

RESULTS AND DISCUSSION

Earlier work indicated that the substrate temperature (Tsub) during CSS deposition played an important role in determining the properties of CdTe films and devices [7]. We have observed that both the grain size and the inner grain quality are strongly enhanced by increasing Tsub. In addition, higher substrate temperatures led to improved device performance with increased open-circuit voltages (Voc). However, we found that as Tsub increased to temperatures above 610°C, material properties continued to improve, but the device Voc decreased sharply. Similarly, the device QE improved as Tsub increased up to 620°C, beyond which degradation was evident. Using a constant substrate temperature throughout the deposition (referred to as the "conventional" profile), the highest efficiency achieved for this sample set was 10.4% [7].

Although "conventional" profiles have produced efficient devices, several critical questions remain unanswered: (i) Can improved material properties, associated with the higher deposition temperatures, be obtained without incurring the detrimental device performance effects? and (ii) Can these results be achieved while maintaining processing temperatures compatible with commercially available low-cost soda-lime glass?
glass (where processing temperatures cannot exceed 600°C for extended periods of time). To help answer these questions, we have developed a novel temperature profiling technique that reduces the total time the substrate remains at high processing temperatures, yet retains many of the benefits associated with the higher processing temperatures (including increased grain growth and improved device performance).

"Conventional" CSS temperature profiles consist of a constant source and substrate temperature throughout the deposition. We find that by adjusting the temperature during the initial stages of deposition, we can strongly influence the film nucleation. Figure 1 shows a modified temperature profile which uses a high-temperature "nucleation" segment \( T_n \) in the initial stages of deposition. Figure 2 is SEM micrographs of CdTe films grown for about 1 minute and nucleated at temperatures of \( T_n = 620°C \) and \( T_n = 645°C \) (Fig. 2a and 2b, respectively). These micrographs clearly show that as the nucleation temperature is increased from 620°C to 645°C, the initial grain size increases and the films become much more faceted (indicating improved crystalline quality). Unfortunately, commercial-grade glass substrates cannot withstand these high processing temperatures for extended periods of time. Therefore, the temperature must be reduced shortly after the peak nucleating temperature is obtained.

To determine if the benefits of a high \( T_n \) could be realized if the bulk of the film is grown at a lower conventional deposition temperature, films were deposited using a variety of nucleating temperatures with profiles similar to the one shown in Fig. 1. Figure 3 shows AFM images of films deposited at a substrate temperature of 600°C, but nucleated at temperatures of \( T_n = 625°C \) and \( T_n = 645°C \) (Fig 3a and 3b, respectively). From these micrographs it is clear that, although the bulk of the film was grown at the same temperature, the \( T_n \) had a significant effect on the final grain size. For about 6-μm-thick films nucleated at 625°C, the average grain size is about 3 μm in diameter. If the nucleating temperature is increased to 645°C, the average grain size increases by a factor of 2, to about 6 μm in diameter.

Device \( V_{OC} \) values are also strongly affected by the deposition temperature, as shown in Fig. 4. We find that using "conventional" temperature profiles (see dashed line in Fig. 4), the device \( V_{OC} \) increases steadily until a substrate temperature of 610°C is obtained. At temperatures in excess of 610°C, the device \( V_{OC} \) decreases rapidly. However, by using a modified temperature profile, similar to that shown in Fig. 1, we can extend the range and increase the maximum \( V_{OC} \). This is shown by the solid line in Fig. 4, where the x axis now indicates the nucleating temperature \( T_n \); the bulk of the film was deposited at \( T_{Sub} = 600°C \). Nucleating temperatures up to about 630°C can now be used before the degradation in \( V_{OC} \) is observed. From these results, it is clear that although the duration of the nucleation segment is short, it has a significant impact on device performance.

On the other hand, we find that when the ratio of the grain size to the film thickness is ≥1, pinholes are often observed. The ratios greater than one are generally
realized at the higher nucleation temperatures for the film thickness around 4 to 6 μm. The increase in the pinhole or "void" density is coupled with a decrease in the device's $V_{OC}$, which substantially reduces device performance. We believe that the voids are introducing shunt paths between the back contact layer and the SnO$_2$/CdS front contact. This would explain the rapid degradation in $V_{OC}$, shown by the solid line in Fig. 4.

![AFM image of CdTe thin films deposited at a substrate temperature of 600°C and nucleated at temperatures of (a) T$_n$ = 625°C, and (b) T$_n$ = 645°C.](image)

Fig. 3. AFM image of CdTe thin films deposited at a substrate temperature of 600°C and nucleated at temperatures of (a) T$_n$ = 625°C, and (b) T$_n$ = 645°C.

To overcome these shunting problems and maintain the benefits associated with the higher nucleation temperature, a low-temperature segment was incorporated into the profile. This low-temperature segment, called the "plugging" temperature (T$_p$), effectively increases the nucleation site density, forming a high density of small grains. Fig. 5 shows a pair of SEM images taken from films nucleated at 645°C and deposited at 600°C, both with and without a 525°C plugging segment. The SEM images reveal that by using a plugging temperature of 500°-550°C immediately after the higher-temperature T$_n$ segment, secondary nucleation sites form and the void density is significantly reduced.

![SEM plane views of CdTe films taken from samples deposited with and without plugging temperature. (a) CdTe film deposited with T$_n$ = 645°C. (b) CdTe film deposited with T$_n$ = 645°C and T$_p$ = 525°C.](image)

Fig. 5. SEM plane views of CdTe films taken from samples deposited with and without plugging temperature. (a) CdTe film deposited with T$_n$ = 645°C. (b) CdTe film deposited with T$_n$ = 645°C and T$_p$ = 525°C.

![Graph showing the device's $V_{OC}$ as a function of nucleation temperature with the bulk of the film deposited at T$_{sub}$ = 600°C (solid line). Dashed line shows the $V_{OC}$'s as a function of constant substrate temperature profile.](image)

Fig. 4. The device's $V_{OC}$ as a function of nucleation temperature with the bulk of the film deposited at T$_{sub}$ = 600°C (solid line). Dashed line shows the $V_{OC}$'s as a function of constant substrate temperature profile.
To maintain the bulk CdTe film quality after depositing the low-temperature "plugging" segment, a third segment was added to the profile. An "annealing" segment ($T_a$) was introduced, resulting in the "two-wave" temperature profile shown in Fig. 6. Using the "two-wave" profile, we realized a significant improvement in device performance as compared to devices produced using the "conventional" constant temperature profile. Fig. 7 shows I-V data from two devices: one where the CdTe layer was deposited using a "conventional" temperature profile and the other deposited using the "two-wave" temperature profile. The $V_{oc}$ and device conversion efficiency increased from 0.774 V and 10.4 % to 0.827 V and 12.0 %, respectively.

**CONCLUSION**

We have demonstrated that by modifying the source and substrate temperature profiles used during deposition, we can maintain the advantages associated with higher substrate temperatures, without suffering the detrimental effects on device performance. Our temperature profiling techniques can be used to grow large-grain material, plug pinholes, and improve device $V_{oc}$ and efficiency. Improved material properties and device performance have been obtained while maintaining deposition temperatures compatible with commercially available substrates. Furthermore, the temperature profiling technique can be easily applied to a manufacturing environment in a technology that is nearing commercialization. Finally, modified temperature profiles have resulted in a 15% increase in device efficiency over devices produced using more conventional temperature profiles.

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**REFERENCES**