A Programmable Power Processor \((P^3)\) has been developed by NASA/Marshall Space Flight Center for application in future large space power systems. The \(P^3\) is capable of operation over a wide range of input voltage (26 to 375 Vdc) and output voltage (24 to 180 Vdc). The peak output power capability is 18 kW (180 V at 100 A). The output characteristics of the \(P^3\) can be programmed to any voltage and/or current level within the limits of the processor and may be controlled as a function of internal or external parameters.

Seven breadboard \(P^3\)s and one "flight-type" engineering model \(P^3\) have been built and tested both individually and in electrical power systems. The programmable feature allows the \(P^3\) to be used in a variety of applications by changing the output characteristics. The tests have been performed for four potential applications, a high voltage battery peak power tracking charger, a 120-V bus regulator, a 30-V bus regulator, and a peak power tracking impedance matching regulator. Test results, including efficiency at various input/output combinations, transient response, and output impedance, are presented. Packaging considerations for the 18 kW are also discussed.

INTRODUCTION

The majority of space power systems utilized by NASA in the 1960's and 1970's were very similar in nature. Typically they were low power, low voltage (22 to 36 Vdc) with the main energy source being primary batteries, fuel cells, solar cell arrays, and, when applicable, a secondary source of Ni-Cd batteries. The largest short duration (1 week to 1 month) power system NASA has designed to date is the Space Shuttle Orbiter electrical power system (EPS) which has a nominal rating of 3360 kW-hr and loads of 25 to 30 kW. The largest NASA long duration EPS was flown on the Skylab and consisted of two nominal 4-kW systems tied in parallel to provide a nominal 8 kW of continuous power at 28 Vdc and supplied approximately 50 kW-hr during its lifetime (1). Both of these systems fall short of the capability that will be required to utilize the opportunities presented for space experimentation, manufacturing in space, power generation in space, and other space activities. The next generation of space power systems is expected to be in the 15 to 100 kW range to support these missions.

One activity which will support these larger systems has grown out of the experience gained from managing and operating the large (at the time) Skylab power system. The Skylab EPS had requirements similar to those expected for the much larger systems of the future. These include requirements for integrating several elements in modular power systems, paralleling separate sources of different characteristics to form a much larger system, and controlling these diverse systems such that no one part of the system is abused or damaged. This was accomplished on Skylab with a significant manned interface and associated cost. The outgrowth of this experience was a desire to design a cost effective, versatile, multipurpose power processor that could be used in a wide variety of power system applications with a minimum manned interface required. A \(P^3\) utilizing a microprocessor based "control" was developed with the capability of providing output voltages of 24 to 180 Vdc at 100 A (18 kW peak) with an input voltage of 26 to 375 Vdc (2). The output characteristics of the \(P^3\) can be programmed to any voltage and/or current within the limits of the processor and may be controlled as a function of several external or internal parameters so that it can function as a battery charger, source maximum power tracker, bus regulator over a wide range of voltages, load sharing regulator, load limiter, etc. The \(P^3\) has been selected in the preliminary EPS design for the Space Platform (SP) being designed to supply a continuous 12.5 kW (expandable to 25 kW) of electrical power for 5 years to the Space Shuttle Orbiter or an assortment of payloads, thus increasing mission duration and/or payload power. This calls for processing twice the power over a life span seven times that of the Skylab EPS.

Seven \(P^3\) breadboards have been built at the Marshall Space Flight Center (MSFC). Four of these are being used in a high voltage SP EPS breadboard at MSFC for system verification testing and analyses; two were supplied to the Johnson Space Center (JSC) for testing to determine their potential application to a Space Shuttle Power Extension Package (PEP), and one is being used at MSFC for further design optimization and testing. Also, one "flight-type" packaged engineering model has been built and tested. Tests to date have verified the performance of the \(P^3\) as a high voltage battery peak power tracking charger, a 120-V bus regulator, a 30-V bus regulator, and a peak power tracking/impedance matching regulator.
The P³ electrical and mechanical design, specific applications, and test results are discussed herein.

**P³ DESIGN**

The P³ is designed to operate with a wide range of input voltages and programmable output voltages with the only constraint being that the input voltage exceed the output voltage by at least 2 Vdc. The output current is also programmable. Total output power capability is 18-kW (180 Vdc at 100 A) peak and 12-kW steady-state. Table 1 gives a summary of the key P³ design parameters and requirements.

**Table 1. Summary of P³ Design Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Level</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTPUT VOLTAGE, Vo</td>
<td>24 TO 180 Vdc</td>
<td>PROGRAMMABLE</td>
</tr>
<tr>
<td>OUTPUT CURRENT, Io</td>
<td>0 TO 100 Adc</td>
<td>PROGRAMMABLE</td>
</tr>
<tr>
<td>INPUT VOLTAGE, Vm</td>
<td>26 TO 375 Vdc</td>
<td>STEADY STATE</td>
</tr>
<tr>
<td>PEAK INPUT VOLTAGE</td>
<td>400 Vdc</td>
<td>LIMITED TO 20 µS</td>
</tr>
<tr>
<td>OUTPUT VOLTAGE RIPPLE</td>
<td>50% OF SL-E-0002A</td>
<td>FOR Vo = 30 Vdc; FOR Vo &gt; 30 Vdc; ALLOWABLE RIPPLE RISES PROPORTIONALLY</td>
</tr>
<tr>
<td>INTERNAL POWER DISSIPATION</td>
<td>600 W</td>
<td>COLDPLATE TEMPERATURE = 30°C</td>
</tr>
<tr>
<td>OVERLOAD PROTECTION, ( I_{oc} )</td>
<td>105 - 115 Adc</td>
<td>HARDWARE IMPLEMENTED; OCCURS WITHIN 10 µS OF OVERLOAD</td>
</tr>
<tr>
<td>OVERVOLTAGE PROTECTION</td>
<td>26 TO 200 Vdc</td>
<td>PROGRAMMABLE</td>
</tr>
<tr>
<td>MAXIMUM STANDBY POWER</td>
<td>140 W</td>
<td></td>
</tr>
</tbody>
</table>

The P³, as shown in the simplified block diagram of Figure 1, consists of two primary elements, the Power Processor (P²) and the Programmable Controller and Interface (PC/I). The PC/I controls the output characteristic of the P² through a digital-to-analog interface by generating an analog voltage which is used as a reference adjust voltage in the P² feedback loop. The design of all elements of the P³ are discussed below.

![Figure 1. P³ simplified block diagram.](image1)

**Power Processor Design**

**Power Stages.** The power stage topology of the P² is the classic "buck" regulator type, shown in Figure 2, with the duty cycle variable from 0 to 100 percent. This topology was chosen for its efficiency in the power processing situations where it was most likely to be used—the unregulated source voltage will be higher than the required output with the input to output voltage ratio typically less than five. We expect these situations to predominate in near-term large space power systems.

![Figure 2. Buck regulator topology.](image2)

High efficiency becomes more critical as space power systems grow in size. In past space applications, the power conversion equipment has not been the primary factor in determining overall structural and heat rejection requirements. A few percent difference in conversion efficiency was of concern but it did not impact the overall structural and thermal designs. A large power system will have kilowatts of conversion losses and a few percentage points in efficiency are significant—regulators processing 100 kW at 92 percent will require 8 kW of heat rejection from a thermal control system whereas 96 percent efficient regulation would only need 4 kW.

The most significant disadvantage of the buck regulator is that a failed regulator can apply input voltage to the output. In applications where this cannot be tolerated even momentarily, the output must be clamped long enough to allow fault clearing elements to activate. In large systems, with multiple regulators per collection bus, one clamp can protect the bus, thus reducing the relative penalty per regulator.

The base drive for the power transistor is derived from a set of supply voltages referenced to the transistor's emitter. A fixed value of drive current is applied to the base when the transistor is on and the base is reverse biased through a low impedance when off. Although not as efficient as a magnetic forced-gain base drive, this technique has the ability to turn the power transistors on 100 percent of the duty cycle and was the controlling factor for this design.

The complete P² has three power stages running synchronized and stagger-phased at 10 kHz. This gives it a regulated output capability of 100 Adc with the peak currents in each power stage limited
to less than 50 A. The synchronized stagger-phasing reduces the maximum combined rms current seen by the input filtering to that which could be demanded by a single power stage. The 10 kHz frequency of each power stage reflects an emphasis on efficiency.

Bias Supply. A bias supply provides all house-keeping voltages, including those required by the base drive circuits. These voltages, particularly those for the control and telemetry functions, must be maintained over a range of input voltage from 21 up to 375 Vdc steady-state with transient excursions outside these limits. This source voltage is converted through a buck-boost pre-regulator to a negative 20 Vdc which is used by a dc to dc converter to drive multiple transformers, as shown in Figure 3. This configuration minimizes cross regulation among the numerous outputs and eliminates the need for post regulation on all higher power outputs except the 5 Vdc logic supply.

![Figure 3. Bias supply.](image)

The pre-regulator and converter power stages are sized to handle up to 175 W. The actual load varies from about 40 to 150 W depending on the base drive requirements.

The negative 20 Vdc is used by the main power stage snubber circuits as a power sink. With an upper range load and low to medium duty cycle requirements, the pre-regulator becomes totally unloaded and a shunt regulator on the 20 Vdc activates to dissipate the excess of power available to the dc to dc converter from the snubber circuits. Thus, the converter processes the entire bias load, and the pre-regulator only makes up the difference between available snubber power and bias requirements.

Filter Banks. The output capacitor bank size was driven more by the need for a good transient response than by output ripple requirements. At voltages of several hundred volts or less, the best volumetric efficiency is available with the wet-slug all-tantalum capacitor. The output bank consists of 9 capacitors of 620 µf at 100 Vdc arranged in a 3 by 3 series-parallel matrix giving 620 µf with a 300 Vdc rating. Derating requirements allowed use of 60 percent of this voltage rating giving the P^2 a 180 Vdc output capability. Each capacitor has a resistor added in parallel to assure voltage sharing so the capacitor leakage currents do not have to be matched. Applications that do not require over 60 Vdc output can take advantage of a large output capacitance by simply rearranging capacitor bus straps to put all 9 capacitors in parallel.

The input capacitor bank design was determined by both transient response and rms current handling capability. Even at twice the voltage requirements of the output bank, the wet-slug all-tantalum capacitors are still the smallest solution. The input bank is a 5 by 3 series-parallel matrix of 460 µf — 125 Vdc capacitors giving 276 µf at a derated voltage of 375 Vdc.

The series-parallel capacitor arrangements have the added advantage that a bank can tolerate any capacitor failing short or open without causing any other capacitors in the bank to see more than rated voltage or currents. This is accomplished without the need for individual capacitor fusing.

Snubber Circuits. The high voltages typically present in the P^2 result in a dominance of transistor switching losses over conduction losses. The switching losses in the P^2 can easily approach 1 kW and their reduction involved a significant portion of the power stage design effort.

Turn-on losses were the most difficult to reduce. Minimizing the peak collector currents required the power inductors to have a larger value such that the power transistor would turn on into an inductor-diode combination that was still conducting. In this circumstance the collector to emitter voltage cannot reduce until the diode has been commutated off. Raising the peak base drive current at turn-on reduces the time needed to commutate the diode but involves higher peak currents. Faster diodes would help but at the required rating these are simply not available. The turn-on snubbing technique implemented is illustrated in Figure 4.

![Figure 4. Power stage snubbing.](image)

The nature of the turn-on waveforms, constant voltage with a fast rising current, suggested that the energy could be stored in a small inductor rather than dissipated in the transistor. This is effective at removing the turn-on losses from the transistor, but the energy now in the inductor must be addressed at turn-off. The negative 20 Vdc of the bias supply provides a convenient sink for this energy. At turn-off the main inductor conducts through the main commutating diode while the snubber
inductor dumps its energy directly to the negative 20 Vdc. This direct energy transfer avoids the problems of magnetic coupling to a secondary winding to get the energy to an isolated load. The power transistor sees an additional 20 Vdc in the voltage it is turning off, but the net dissipation reduction is significant.

The commutating diode still has to face some excess energy that was stored in the parasitic and snubber inductances because it required some reverse current to be commutated. Without the addition of the snubber inductor, this energy is smaller, and its effects are attenuated by the collector to emitter capacitance of the power transistor. With the snubber inductor in the circuit, the diode is isolated from that protective parasitic capacitance, and it is necessary to add a small capacitor across the diode. The magnetic coupling was necessary in this case because there was no convenient load referenced to the positive input power. Snubbing turn-on losses this way is very effective until the duty cycle approaches 100 percent, requiring the power transistor to turn on again before the snubber inductor has finished dumping to the negative 20 Vdc. However, this only occurs when the input voltage is lowered to just above the required output, and the turn-on losses incurred are acceptable as a result of the lower voltage.

The turn-off loss characteristic, constant current with a fast rising voltage, lends itself to capacitive snubbing. A capacitor reduces the turn-off losses in the transistor, but to reduce the net losses a non-dissipative method for resetting the capacitor was designed. The turn-off snubber circuit shown in Figure 4 accomplishes this. In its most direct application, this circuit would be placed across the main power diode. However, when both snubber circuits are combined, it is more effective to put the turn-off snubber circuit across the commutating diode in the turn-on snubber as shown. While the diode is conducting, both capacitors will be discharged. When the power transistor is turned on, the two capacitors and inductor form a series LC circuit which resonates both capacitors up to the input voltage. The peak voltage is held by the diode, and the capacitors are ready to snub the next transistor turn-off.

Pulse Width Modulation (PWM) Control. The power stage on-times are initiated by synchronized stagger-phase start pulses derived from a ring counter. After turn-on a separate circuit for each power stage determines how long the power transistor should stay on. This pulse width is normally determined by one of two selectable modes. The \( V_0 \) mode regulates the output voltage, and the \( V_0/V_{\text{Vin}} \) mode allows the PC/I to directly control the pulse width.

The \( V_0 \) mode PWM is implemented by the common practice of comparing a ramp voltage to an error signal. The ramp voltage has a variable slope proportional to the input voltage. This has the advantage of making stability in the error signal generation independent of the wide range of input voltage. The error signal is derived from an integrating feedback loop that looks at the actual output and a primary reference voltage (PRV) provided by the PC/I. The feedback loop is compensated to provide fast stable transient response. Current sharing between the power stages is accomplished by adding a signal proportional to the current in the corresponding power inductor to each ramp. Thus, higher currents reduce the on-times creating a resistive effect without the equivalent power losses.

Fast response voltage regulators inherently have a negative impedance characteristic at their inputs and require a low impedance power source to perform properly. The negative input impedance characteristic may cause instability when the source has a high impedance, such as a solar array operating near its peak power point which is typical for a battery charger. To deal with this problem a control method which has the PRV directly in control of the duty cycle was developed. This causes the power stages to behave like dc transformers in which the PC/I has control over the turns ratio or the \( V_0/V_{\text{Vin}} \) value. This \( V_0/V_{\text{Vin}} \) mode was incorporated by using analog switches to reconfigure the circuit elements already present for the \( V_0 \) mode. The proportional ramp was given a fixed reference, and the PRV was used to compare against that ramp to give the PC/I direct control over the power stage duty cycle. The signal proportional to power inductor current was left in the ramp so there would still be load sharing between power stages. The feedback amplifier has no nominal active control task in this mode, but it is used to provide a fast responding voltage limit by being given a fixed reference instead of the PRV. This is required under light loading conditions with discontinuous current in the power inductors when the \( V_0/V_{\text{Vin}} \) ratio can reduce to unity regardless of programmed duty cycle. This could cause high voltage on the output before the PC/I could respond if fast analog limiting were not provided.

A third PWM control mode is based on sensing and limiting peak current in the power inductors to protect the power semiconductors. This mode controls the peak stresses in the power stages under fault conditions to acceptable levels until the PC/I can react by changing the PRV or deactivating the power stages. Although the stresses are controlled they can be very dissipative, and the \( P^2 \) is not designed to sustain them indefinitely, primarily because of thermal constraints. Figure 5 shows how all three control modes are implemented using common circuit elements where feasible.

The pulse width duration drive must be made available to the base drive circuits referenced to the power transistor emitters. This is done magnetically with two pulse transformers, each of which is active on alternate power cycles. Since each pulse transformer is capable of over 50 percent duty cycle, the combination can be overlapped to give 100 percent duty cycle at the power transistors.

Current Signal Conditioning. The PWM circuits of each power stage require wide bandwidth current signals that will maintain their fidelity from dc
The memory section is composed of both read-only-memory (ROM) and read/write memory (commonly called RAM) devices. The ROM consists of four bipolar integrated circuits (ICs), each having $2K \times 8$ ($K = 1024$) bits of memory space arranged to produce an $8K \times 16$ bit program memory space. The RAM consists of twelve MOS ICs, each having $256 \times 4$ bits of memory space, arranged to produce a $768 \times 16$ bit read/write memory space. Also included are 54LS devices used to implement the CPU to memory interface.

The I/O section is composed of two, sixteen channel analog multiplexers, a 12 bit analog-to-digital (A/D) converter, a 12 bit digital-to-analog (D/A) converter, four discrete digital inputs, one discrete digital output, one discrete digital output, 54LS devices for interfacing to the CPU, and the signal conditioning circuitry for the analog inputs. One of the multiplexers is used to insure proper operation of the D/A and A/D converters via a self-test software procedure and the other is used to connect one of 16 analog inputs to the A/D converter during normal operation. The output of the A/D converter and the input to the D/A converter are connected to the CPU data bus through the interface devices. The output of the D/A converter is the primary reference voltage (PRV) through which the PC/I exercises its main control of the F^3. Three of the four discrete digital inputs are latched commands, meaning that their last commanded state remains even during a power interruption. The fourth input is a signal from the F^2 indicating a current limit condition. The discrete digital output is only an extension of the F^3 on/off status input. The function of the signal conditioning circuitry is to provide the proper isolation and ranging for the analog inputs. Certain of these ranges are a function of connections on the patch plug connector.

The C/D section is composed mainly of 54LS type devices through which the CPU can communicate with either a Flexible Multiplexer/Demultiplexer (FMDM) interface, which is the standard Space Shuttle interface, or a Remote Interface Unit (RIU), which is part of the NASA Standard Telemetry and Command Components (STACC) Interface group. Either the FMDM or RIU C/D interface is selected by inserting the desired printed circuit card and making the necessary external connections.

PC/I Operation. The basic function of the PC/I is to sample the analog and digital inputs, insert these and the command adjustable parameters (CAPs) into its programmed control algorithms, and determine which direction and how much to move the PRV. A CAP is a parameter, initialized in RAM to a preprogrammed value stored in ROM, which can be examined and/or changed via the C/D interface.
CPU to perform any required functions on a real-time basis. The time delay interrupt signals the CPU that a programmed time has elapsed since the timer was initialized, and is used to allow the P3 time to respond to a PRV update before certain analog signals are sampled.

**Mechanical Configuration and Design**

The P3 package configuration, as shown in the mechanical outline drawing of Figure 6, consists of the power stage section (with separate cavities for each stage) and four modules containing the bias supply, the microprocessor and associated memory, the input/output circuitry, and the command and data interface. This configuration was selected based on the requirement for repairability and replacement of major components and on two key design drivers: semiconductor junction temperatures and EMI.

The basic mechanical design of the P3 was driven by the need to limit the junction temperatures of the main power stage transistors. The dissipation in each junction exceeds 200 W at maximum load, thus requiring low thermal resistance from case to heat sink as well as from junction to case. This requirement was met by mounting the power transistors and the commutating diodes directly on the cold plate mounted base of the package. Total continuous thermal dissipation of the package design without exceeding components ratings is 600 W at a coldplate temperature of 30°C.

The power processor layout design concentrated on reducing EMI to minimize the need for filtering between the P2 and PC/I interfaces. The current loop with the highest di/dt component, and thus the major source of di/dt EMI, is the path between the input capacitors, the switching transistor, and the commutating diode. The source of the highest dv/dt EMI is the base drive circuitry which is referenced to the emitter of the switching transistor. To reduce the EMI, major efforts were made to minimize the length of the loops in these two areas. The results of these efforts were the concentration of the components of each power stage in a separate cavity.

The assembled "flight-type" engineering model is shown in Figure 7. The input and output power is connected through two 4-pin connectors mounted on the upper front. The signal and patch plug connectors are mounted on the back of the rear module, and the analog measurement connector is mounted on the side of the rear module. The total package weight is 72 lb with a volume of approximately 1.17 ft³.
The primary unique feature of the P³ is its flexibility and applicability to the various functions which must be performed in a space power system. With only the selection of the proper ROM in the P³ microcomputer required, any one of the operating modes listed in Table 2 can be selected. Software for these operational modes currently exists. The effort required to add additional operating modes is the software development for the particular mode desired. However, savings in software development for the additional modes is possible because of the system-level software already developed for the current operating modes. This system-level software includes the command data software, analog-to-digital (A/D) and digital-to-analog (D/A) control, and the basic operating structure. In most cases, the system-level software is applicable to any new algorithm development.

Table 2. P³ Programmable Operating Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery Charger/PEAK Power</td>
<td>Battery Ampere-hour Integration</td>
</tr>
<tr>
<td>Tracking</td>
<td>Battery Temperature &amp; Current Compensated</td>
</tr>
<tr>
<td></td>
<td>Voltage Control</td>
</tr>
<tr>
<td>Solar Array PEAK Power</td>
<td>Solar Array PEAK Power Tracking</td>
</tr>
<tr>
<td>Tracking</td>
<td>CAUTION AND SHUTDOWN</td>
</tr>
<tr>
<td>Matching Regulator</td>
<td>Voltage Regulation (24V to 180V)</td>
</tr>
<tr>
<td></td>
<td>PROGRAMMABLE OUTPUT RESISTANCE</td>
</tr>
<tr>
<td></td>
<td>BPRC CONTROL</td>
</tr>
<tr>
<td></td>
<td>CAUTION AND SHUTDOWN</td>
</tr>
<tr>
<td>High and Low Voltage Bus</td>
<td>Voltage Regulation (24V to 180V)</td>
</tr>
<tr>
<td>Regulator</td>
<td>PROGRAMMABLE OUTPUT RESISTANCE</td>
</tr>
<tr>
<td></td>
<td>BPRC CONTROL</td>
</tr>
<tr>
<td></td>
<td>CAUTION AND SHUTDOWN</td>
</tr>
<tr>
<td>Peak Power Tracker/Impedance</td>
<td>REGULATE FUEL CELL OUTPUT POWER</td>
</tr>
<tr>
<td>Matching Regulator</td>
<td>PEAK POWER TRACKING</td>
</tr>
<tr>
<td></td>
<td>CONTROLLED LOAD SHARING</td>
</tr>
<tr>
<td></td>
<td>CAUTION AND SHUTDOWN</td>
</tr>
</tbody>
</table>

Bus Voltage Regulator

The P³ can be programmed to regulate its output voltage (Vo) and current (Io) to any value within the specification limits. Optimum performance at a particular Vo could also require ranging the Vo telemetry and PRV signals and connecting the output filter capacitors in the proper configuration. Ranging is optional, but would be done (via software or patch plug connections) to give the PC/I greater resolution in controlling Vo over the smaller range.

A minimum requirement of a bus voltage regulator is to share power with other regulators on the same bus. This can be accomplished by programming a drop in Vo that is proportional to Io, or what is commonly called load slope multiplier, and CAP indicating the parameter is command adjustable. This technique has been demonstrated at MSFC with two bus voltage regulator P³s.

Many applications for a bus voltage regulator receive input power from a nickel-cadmium (Ni-Cad) battery. The use of Ni-Cad batteries often requires that precautions be taken to prevent any cell from collapsing and becoming reverse-biased, which would result in cell damage and possible loss of the battery. A device to preclude this has been developed at MSFC and is known as a Battery Protection and Reconditioning Circuit (BPRC) which is basically a dc to dc converter with a separate low voltage output for each cell (4,5). If a cell becomes weak and collapses, the BPRC output will maintain a positive voltage on the cell, but since the capabilities of the BPRC are limited, the bus voltage regulator must reduce the amount of power drawn from the battery to maintain cell protection if several cells collapse simultaneously. Algorithms developed and demonstrated at MSFC incorporate a three-fold response to the BPRC input current (which is a direct indication of the state of the cells). The PC/I will (1) control the P² in reducing the load at a rate proportional to the rise in BPRC input current; (2) turn the P² off if the BPRC input current is abnormally high (fast response) and then back on at a minimum power level; and (3) maintain the BPRC input current at a constant level. A digital filtering technique for the BPRC input current is also used in these algorithms.

V³/V³⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻{-}
normal analog inputs and outputs. It also required a command to select which unit should act as the master.

The configuration was tested extensively and performed very well in the nominal system configuration. The limiting factor that would back the units out of peak power tracking was the remotely sensed fuel cell voltage. This voltage limit was selected to leave a residual load on the fuel cell that helped it maintain an acceptable standby condition. The voltage limit required was expected to change as the fuel cell aged, and the ability to change the programmed limit with a simple command was very convenient.

A P3 in a charger function also has a role to play in the BPRC current control scheme discussed earlier under the bus regulator application. As explained there, the BPRC is useful in protecting weak cells in NiCad batteries from voltage reversal but requires a reduction in battery load if several cells need assistance. If the load is reduced far enough, it is possible to assist all cells in a battery and to hold them at less than 0.8V per cell. If this state is maintained for an extended period, a reconditioning of the battery cells is accomplished. Performing such a reconditioning of the battery cells is very desirable in long life applications. A disadvantage of this action is that, unless the corresponding solar array can be made available to other chargers, its power output is not available to the system. Here is where a "smarter" charger can be of use. The P3 charger can be programmed to also look at the BPRC current during battery reconditioning and increase its power output if the current goes above a certain limit. If the limit the charger uses is slightly below what the regulator is responding to, then the net effect is the regulator will deliver normal load output during solar array illumination. When the solar array is occulted and the charger cannot maintain the BPRC current below its limit, the regulator will respond by reducing its load. Thus, a significant portion of that solar array's power will be delivered to the system, even while the battery is being conditioned. This technique has been successfully tested at MSFC using breadboards of the BPRC, P3 regulator, P3 charger, and a battery.

**P3 TEST RESULTS**

**P3 Parametric Testing**

Parametric testing at representative input and output conditions was conducted on a P3 breadboard at MSFC (6). This testing included efficiency, output impedance (Zo), transient, and gain and phase (G/P) margin measurements. The efficiency measurements have been adjusted to reflect the known differences between the breadboard P3, which has lower standby losses, and the proposed "flight-type" P3. The Zo, transient, and G/P margin measurements should be the same in either version. A sample of these measurements has been included here.

**Efficiency.** Efficiency measurements on the P3 were all taken with the 3 x 3 output filter configuration. The efficiency measurements at Vo = 30 and 120 Vdc and Vin = 150 and 375 Vdc are shown in Figure 8.

![Figure 8. P3 efficiency.](image)

**Output Impedance.** The Zo measurements are shown in Figures 9 and 10. These measurements were taken by inducing a 6A peak-to-peak (P-P) sine-wave current on the P3 output, measuring the resulting P-P change in Vo, and then dividing Vo(P-P) by Io(P-P). The peak on each graph is a function of the resonant frequency of the main inductors, the output filter bank, and the internal feedback circuitry. The only condition affecting the value of Zo at a particular Vo was whether or not there was sufficient loading for continuous current in the main inductors.

**Transients.** Figures 11, 12, 13, and 14 show a sample of the transient test waveforms. The transient tests were conducted by switching resistive loads of the magnitude indicated on the P3 output. All transient tests were at Vin = 150 Vdc.

**Gain/Phase Margins.** The G/P margin measurements are listed in Table 3. The measurements were taken by inducing a small sine-wave perturbation into the internal feedback circuitry of the P2 control and measuring the gains and phase shifts.
Engineering Model Testing

The engineering model testing to date was performed by Martin Marietta Aerospace and includes acceptance and qualification level testing. The goal of the P³ engineering mode test program was to demonstrate the basic capability and adequacy of P³ to meet the design requirements. In most cases, tests that were not initially compliant with the specification limits were rerun after a modification to the P³ and retested successfully, but there were a few situations where the necessary modifications could not be made immediately due to budget constraints. Table 4 reflects the qualification level testing performed. Test results were encouraging, but there are areas where minor changes and retest will be performed when additional funds are available.

CONCLUSION

The P³ development presented herein has demonstrated several technologies vital to future large space power systems: high voltage, high power operation; programmable operating characteristics; and interface capability to function in automated power systems, thus reducing ground control costs. The desirability of these capabilities are clearly
Table 4. $P^3$ Engineering Model Qualification Level Testing

1. ELECTROMAGNETIC COMPATIBILITY PER SL-E-0002A

2. VIBRATION TESTING, RANDOM
   (a) Z AXIS – 20 GRMS 2.0 KHz
   (b) X AND Y AXIS – 10 GRMS 2.0 KHz
   (c) VEHICLE DYNAMICS SINE

3. THERMAL VACUUM TESTING
   (a) -20°C TO +30°C BASE PLATE TEMPERATURE
   (b) 5 CYCLES – 4 HOURS EACH

indicated by the acceptance shown through four potential applications currently considering the $P^3$. Since the cost of development of a large power processor of this type is approximately $2M, this represents a potential savings of $6M. Further savings on reduced ground operations and other potential applications can be anticipated.

REFERENCES


Table 3. Typical $P^3$ Gain/Phase Margins

<table>
<thead>
<tr>
<th>Vin</th>
<th>Vo</th>
<th>Io</th>
<th>GAIN MARGIN (db)</th>
<th>PHASE MARGIN (DEG)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>30</td>
<td>20</td>
<td>13</td>
<td>38</td>
</tr>
<tr>
<td>150</td>
<td>30</td>
<td>50</td>
<td>13</td>
<td>41</td>
</tr>
<tr>
<td>300</td>
<td>30</td>
<td>50</td>
<td>14</td>
<td>44</td>
</tr>
<tr>
<td>150</td>
<td>120</td>
<td>17</td>
<td>7</td>
<td>45</td>
</tr>
<tr>
<td>150</td>
<td>120</td>
<td>49</td>
<td>6</td>
<td>40</td>
</tr>
<tr>
<td>300</td>
<td>120</td>
<td>49</td>
<td>8</td>
<td>35</td>
</tr>
</tbody>
</table>