A Readout System for High-Speed CCD Cameras Based on Advanced Telecommunications Computing Architecture

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Abstract—This paper describes the performance of a scalable readout system for high-speed CCD sensors based on the Advanced Telecommunication Computing Architecture specification. The paper reports the readout system performance tested with a 1MPixel Frame Store CCD sensor for soft X-ray applications at synchrotron light sources. This camera is capable of producing image data at over 400 MB/s which must be processed in real-time and stored to disk. The high-level hardware architecture, signal processing data flow, and network protocol optimization are also be presented.

I. INTRODUCTION

The rapidly increasing data rate of X-ray pixel sensors developed in collaboration between Lawrence Berkeley National Laboratory (LBNL) and Argon National Laboratory (ANL) has necessitated the development of a highly scalable and fast CCD data acquisition system. The current target camera head is a 1 Megapixel CCD based soft X-ray camera (1kFSCCD), which operates up to 200 frames per second [1]. This camera head produces a continuous stream of raw data at a rate greater than 400 MB/s, which outpaces most CCD data acquisition architectures [2][3]. To meet this challenge and to prepare for the next generation of CCD camera head, a scalable CCD readout system has been developed based on the PICMG 3.1 Advanced Telecommunications Computing Architecture (ATCA) specification.

The PICMG 3.0 ATCA specification was developed by a consortium of 250 companies to standardize a highly reliable and compact architecture for high-speed real-time packet switching and computing for telecommunications equipment. The PICMG 3.1 ATCA further specifies the protocol of the ATCA backplane as redundant 10 Gigabit Ethernet, which is currently the de facto standard among manufacturers of compliant equipment. The fast CCD camera readout system is based on the PICMG 3.1 specification but deviates with the addition of a non-compliant custom camera interface front board and the removal of the redundancy requirement in order to double the available bandwidth on the backplane.

II. READOUT SYSTEM DESCRIPTION

The fast CCD camera readout system was designed around widely accepted commercial standards to minimize development time and to take advantage of the wide array of compatible commercial components. The backbone of the readout system is built on two private networks one reserved for data transport and the other reserved for control and configuration of resources. The data transport network is built on bidirectional 10 gigabit Ethernet with a dual star topology. Nodes on the network include a camera interface node (CIN), user interface node, one or more storage nodes, and zero or more data processing nodes. The current readout system for the 1kFSCCD camera head implemented the simplest complete readout system in this framework with only three nodes a CIN, a user interface node, and a storage node (see Figure 1 and 2).

Figure 1 – An ATCA based 1kFSCCD camera head readout system.

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The 1kFSCCD camera head consists of four printed circuit boards: a top board which carries the backside illuminated CCD, a clock board which drives the CCD clocks and depletion voltage, and two data module boards which hold six FCRIC2 8-channel pipeline ADCs each. The camera head is connected to the CIN though mezzanine camera head interface modules which allow for customization of the cabling. There are currently two versions of the modules, one for LVDS over copper cables and one for high-speed optical transceivers for serialized fiber cables.

The only custom hardware component in the ATCA readout system is the CIN which is a full ATCA front board that interfaces the camera head to the data transport and configuration and control networks (see Figure 3). The CIN consists of three mezzanine camera head interface modules: a large Xilinx Virtex-6 FPGA with 16 MB of SRAM for image processing, camera head control, and data packetization; a small Xilinx Spartan-3 FPGA for configuration and control as well as remotely updating firmware; and front panel input and output triggers for synchronizing the X-ray camera with experimental setups.

Real-time control of the camera head is implemented in the CCD Control and Processing FPGA on the CIN (see Figure 4). Timing waveforms for the CCD clocks and digitizers are generated with a synchronous Finite State Machine FSM in firmware. Data from the camera head digitizer modules is aligned and read into the FPGA where it is fed into an image processing firmware block. This block is still under development and will take over many of the functions currently implemented in software on the user interface node such as dark image subtraction, hot pixel suppression, gain correction, and data compression.

After processing, data on CIN is packetized for transmission to other nodes on the data transport network. Data is currently transported using the User Datagram Protocol (UDP) which is simple but lossy. UDP streaming will be replaced by TCP streaming and streamed directly to storage node using Internet Small Computer System Interface (iSCSI) protocol.

A prototype ATCA readout system has been used to capture X-ray data with a 1kFSCCD camera head at the LBNL Advanced Light Source (ALS). The system included a ATCA processor blade running the user interface software and preformed image descrambling, image formatting, and iSCSI write operation to the storage node. All three tasks will soon be implemented in firmware on the CIN. Images were written to disk in uncompressed 16-bit grayscale Tagged Image File Format (TIFF).

Benchmarking the nodes on the data transport network showed that the CIN was capable of saturating a 10 gigabit Ethernet link with jumbo UDP packets which translates to a payload data rate of 9.8 gigabits per second. While the ATCA backplane is highly reliable the UDP protocol does not guarantee packet delivery and data packets were dropped in the processor blade ring buffer. Tuning the network interface parameters and multi-threading the interrupt servicing routine on the processor blade increased the sustainable data rate significantly.

III. EXPERIMENTAL RESULTS

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Benchmarks were also recorded for sustained write bandwidths from a processor node emulating the CIN direct write firmware to a storage node (see Figure 5). The processor blade was a Kontron AT8050 running Scientific Linux 6.2. The CIN firmware was emulated with direct data write Linux command line tools and all system buffers were cleared to verify data transmission was complete. The storage node was a SANBlaze Technology, Inc. SB-ATCA200 ATCA 10GbE IP-Storage RAID Blade with SEAGATE ST91000640SS 7200 RPM Constellation2 hard drives. Hardware iSCSI 64 kilobyte striped RAID0 targets were created on the storage. Bandwidths are reported for a single RAID0 configuration using all available drives, for a dual identical RAID0 configuration with half the drives in each, and a theoretical bound which is bandwidth sum of the individual drives used in the RAIDs.

![Figure 5 – Storage node bench marks.](image)

**IV. REMARKS AND CONCLUSIONS**

In this paper we presented a new X-ray camera readout system that has been built at the Lawrence Berkeley National Laboratory. This system builds on the ATCA specifications and is highly scalable through the addition resource nodes such as process and storage.

Completing the firmware development implementing TCP data streaming and iSCSI direct to disk streaming on the CIN will transition the systems from the prototype phase to production. Further development will implement additional image processing and compression algorithms to reduce data storage requirements.

**REFERENCES**

