Alumina, Al$_2$O$_3$, Layers as Effective P-Stops for Silicon Radiation Detectors

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Abstract—Inter-strip shortening due to electron accumulation is a problem for any segmented p-type and double-sided n-type detectors. The standard approach for inter-strip or interpixel isolation is an implanted and annealed p-type layer, called p-stop. We show that alumina layer can be used as effective p-stops due to a negative surface charge at the silicon-alumina interface. We used ALD (atomic layer deposition) and e-beam evaporated alumina layers as inter-strip dielectrics for n-on-n strips. We fabricated a double sided strip detector (DSSD) on n-type silicon with alumina as a p-stop and tested the DSSD under gamma-ray irradiation. We compare ALD alumina layers with standard silicon oxide for isolating n-on-n strips. Equivalents to “p-stop” and “p-spray” were fabricated and evaluated with respect to their leakage currents. Finite element simulations support our experimental findings.

I. INTRODUCTION

The most common insulator for silicon based radiation detectors is silicon-oxide, SiO$_2$. The interface between a SiO$_2$ layer and the bulk silicon develops a layer of fixed charge. This charge, which is present to some degree even prior to irradiation, is normally positive. The presence of this layer induces an inversion layer of the opposite charge (called an accumulation layer in the case of electrons) which remains permanently attracted to it from the bulk. The accumulation layer can compromise the isolation of implants on the n-side of strip and pixel devices unless special isolation features are implemented. The electron accumulation can ultimately short the n-implants. The most common techniques to maintain implant isolation are: p-stop [1] and p-spray [2] techniques, see Fig. (1). P-stops are implanted p$^+$ channels between neighboring n-implants. A p-spray layer is a shallow p-type implant that is applied across the full wafer without mask prior to any other processing. The dopant concentration of the implant is matched to the interface charge. However, the p-sprays and p-stops have the drawback of adding a mask level to the fabrication process that increases its complexity and cost. Furthermore, the high electric fields at the edge of the p-stops have been shown to induce pre-breakdown micro-discharges which decrease the signal-to-noise ratio [3].

In this paper we show that it is possible to replace the silicon oxide with an ALD (atomic layer deposition) alumina, Al$_2$O$_3$ layer. Properly treated Al$_2$O$_3$ layers can form negative charges at the silicon interface with densities of $\sim 10^{13}$ cm$^{-2}$. (The negative surface charge is used in the solar cell industry to increase carrier life times [4].) A negative interface charge with silicon is quite unique; commonly used dielectrics in semiconductor processing, e.g. silicon oxide and silicon nitride, have positive interface charges. When an alumina layer is deposited on silicon, the negative interface charge acts like an effective p-stop.

II. CONCEPT AND SIMULATIONS

Fig. (2) shows a schematic of an alumina layer as an effective p-stop. Since there is a negative interface charge present at silicon-alumina interface, no electron accumulation can form underneath the interstrip dielectric. The alumina can be deposited using ALD during regular sensor fabrication or in “post-processing” because ALD is a low-temperature process.

Fig. 1. Schematics of p-stop and p-spray interstrip isolations of n-strip on p-type Si.

Fig. 2. Schematics of an alumina layer as an effective p-stop layer. The negative interface charge isolates the n-strips.

The existence of negative fixed charge between Al$_2$O$_3$ and Si interface is caused by the negatively charged Al ions with a tetrahedral coordination contacting to the silicon atoms of the
interface [5]. The interface charge density depends on the deposition method for the alumina. Thermal and plasma assisted ALD alumina layers have a negative interface charge. Furthermore, the charge can be changed with an annealing step. ALD is the most common deposition method because it can be done at low temperature < 350 °C, and the deposition leads to an absolute conformal coating. The low deposition temperature makes ALD acceptable for processing finished silicon sensors with metallization. (For fully processed silicon sensors, temperatures must be kept below 450 °C to protect the topside metallization.)

Beside the interface charge, the interface trap density is also important as an interstrip dielectric. ALD deposited alumina, on either n- or p-type Si, has an extremely low trap density. This is a unique feature for a low-temperature process. A silicon oxide can have a low trap density when the film is thermally grown at high temperatures. The cause for the low trap density is still under investigation. Dingemans et al. claim that the ALD deposition reactions provide elemental hydrogen at the interface for defect passivation [6].

Finite element (FEM) simulations are carried out with the Atlas Device Simulation software package, produced by Silvaco International. Atlas is a 2-D simulator software, thus, it is important to simulate cross-sections in which the variations of the physical quantities in the third dimension are negligible. All the simulations are performed solving both the Poisson’s equation and the carrier continuity equations. In this way, it is possible to have a complete description of the system in terms of electrical quantities (potential and electric field distributions, carrier distributions and current densities).

Fig. (3) shows a FEM simulation of the electron distribution for an oxidized n-type silicon substrate (2,000 Ωcm). The positive charge (10^11 cm^-2) leads to an electron accumulation at the silicon/silicon oxide interface.

Fig. 3. FEM simulation of electron concentration underneath a SiO2 layer (substrate high resistivity n-type Si).

Properly treated Al2O3 layers can form negative charges at the silicon interface with densities of ~ 10^{11}-10^{13} cm^-2 [4]. Fig. (4) shows a FEM simulation of the electron distribution for an alumina layer n-type silicon substrate (2,000 Ωcm). The negative charge (10^11 cm^-2) “pushes” the electrons away from the interface, providing an effective p-stop layer for inter-strip isolation.

Fig. 4. FEM simulation of electron concentration underneath an alumina layer (substrate high resistivity n-type Si).

We simulated the resistivity values for alumina and SiO2 interstrip isolations as a function of the interface charge, see Fig. (5). The resistivity for alumina is orders of magnitude higher than for SiO2. Furthermore, the value of the resistivity for alumina does not significantly change with the charge density. The resistivity of SiO2, on the other hand, changes with the charge density. This is a well-known phenomenon for radiation sensors. A thermally grow oxide has a charge density of ~ 10^{10}-10^{11} cm^-2. Under irradiation the positive interface of the oxide can change by up to 2 orders of magnitude, maxing out at ~10^{12} cm^-2. Since the resistivity curve for alumina is effectively flat, we assume that an interface charge change induced by irradiation will not compromise the effectiveness of the alumina as a p-stop. (This still needs to be confirmed experimentally.)

Fig. 5. FEM simulations of the resistivity values between two n-on-n strip with a 50 μm gap for alumina and silicon oxide as a function of the interface charge (fully depleted, 20 kΩcm n-type substrate).
III. MICROFABRICATION

We tested alumina layers as effective p-stops by fabricating DSSD on n-type silicon (4” wafers, 0.5 mm thickness, substrate resistivity 20 kΩcm). Fig. (6) shows a simplified process sequence (no cleaning steps are shown). We performed standard cleaning procedures before any high temperature process steps. The wafers were thermally oxidized. We opened the oxide mask on front and back side with RIE (reactive ion etching) steps. The contacts were defined by ion implantation steps: (i) front side boron (p-on-n strips): dose $1.5 \times 10^{14}$ cm$^{-2}$ and energy 50 keV, (ii) back side phosphorous (n-on-n strips): dose $1 \times 10^{14}$ cm$^{-2}$ and energy 75 keV. The implants were annealed for 20 min at 950 °C. After annealing the back side oxide for the n-on-n strips was partially removed by a RIE etch step. (The partial oxide removal ensures that we have devices with oxide and alumina as interstrip isolations on the same wafer.) We deposited 80 nm of alumina by thermal ALD (system: Oxford Instruments FlexALD) at 300 °C after a 10 seconds BOE (buffered oxide etch) step. Trimethylaluminum, Al(CH$_3$)$_3$, (TMA) and water, H$_2$O, were used as precursors for the aluminum oxide. The BOE step ensures that the silicon surface has a hydrogen termination. The excess alumina was removed by a RIE etch step using a CF$_4$ plasma chemistry. After the RIE step the wafers were annealed at 300 °C for 10 min. Aluminum metal contacts were deposited on the front and back side by e-beam evaporation.

Fig. 6. Simplified process sequence (no cleaning steps shown).

We used thermal ALD depositions for the sensors that were tested under gamma-ray irradiation. Some sensors for interstrip isolation measurements were made with an e-beam evaporated alumina layer. We did a 10 seconds BOE (buffered oxide etch) step before we performed the e-beam evaporation.

The strip dimensions were 0.85 x 7.1 mm. The DSSD had 10 front and back side strips with a multi ring guard ring structure on the front side and a single guard on the back side. The strip gap was 50 µm.

Since we removed the oxide only partially between the strips, we can make “p-spray” and “p-stop” types of devices, see Fig. (7). Fig. (8) shows an optical micrograph of a “p-stop” sensor. The area of high electric field will vary by the type of device. For the “p-stop” like of devices, the high electric filed will be located where the alumina and SiO$_2$ dielectric meet.

IV. DEVICE TESTING

The effect of the alumina was tested with a standard probe station. We measured the strip-to-strip (n-on-n strips) resistivity, see Fig. (9) for a schematic.

Fig. 9. Measurement of interstrip resistivity.

Fig. (10) shows the IVs curves for strips with alumina (“p-spray” type of devices) and SiO$_2$ inter-strip dielectrics. The conductivity for the silicon oxide layer is much higher due to the electron layer underneath the oxide (measured resistivities: SiO$_2$ $3 \times 10^6$ Ωcm$^{-2}$ v. Al$_2$O$_3$ $1 \times 10^9$ Ωcm$^{-2}$).

Fig. 10. IV curves for a thermally grown silicon oxide and a thermal ALD deposited alumina as an inter-strip dielectric (n-on-n strips).
An alternative method deposition for alumina is e-beam evaporation [5]. E-beam evaporated alumina layers also have a negative interface charge. The interface charge density can be changed by annealing in an inert gas environment. We annealed the sample for 30 min at 350 °C in an argon environment. Fig. (11) shows the IV’s curves for strips with alumina (“p-spray” type of devices) and silicon oxide inter-strip dielectrics. As for the ALD deposited alumina, the conductivity between two n-on-n strips is dramatically reduced. Although, the direct comparison of ALD and e-beam evaporated alumina shows, see Fig. (12), that the current for alumina is significantly lower. Furthermore, Fig. (12) shows the effect of the annealing step.

We measured the leakage currents of the devices using a probe station at room temperature. The IV curves were collected by using a Keithley 237 high voltage source measurement unit. Fig. (13) shows the IV’s curves for currents for “p-stop” and “p-spray” type of devices. The slope of the curves does depend on the type of alumina stop. This could be caused by different breakdown at the edge of the alumina layer. The critical region from the breakdown point of view is localized (i) at the intersection of the n implant and the alumina for the “p-spray” type of sensors and (ii) at the intersection of the silicon oxide and alumina for the “p-stop” type of sensors. The avalanche is caused by the potential difference forced between these two regions which, in turn, depends on the applied bias voltage [3].

We collected spectra with a Co-57 gamma-ray source with an Amptek Pocket MAC (model 8000A). The HV-power supply was a Silena Model 7716. The shaper was an Ortec 570 (collection time 0.5 μsec). We used sensors with alumina (“p-spray” type) and silicon oxide as interstrip dielectrics. The sensors originated from the same wafer. All spectra were collected at a bias of -120 V (full depletion at -90 to -100 V). The high voltage was applied at the p-on-n side. We collected spectra from the electron and hole signals, see Figs. (14-17).
Fig. 15. Co-57 spectra taken with a sensor with SiO₂ as an interstrip dielectric for the n-on-n strips.

Fig. 16. 122 keV peak from a Co-57 spectra taken with a sensor with Al₂O₃ collecting electrons on with a p-on-n strip.

Fig. 17. 122 keV peak from Co-57 spectra taken with a sensor with Al₂O₃ as an interstrip dielectric n-on-n strips.

Fig. (14) shows the 122 keV peak from Co-57. These spectra were collected with a silicon oxide as an interstrip dielectric for the n-on-n side. The 122 keV peak is clearly detectable for the electron signal on the p-on-n side. When we switched to the n-on-n side, the signal was noisy, no 122 keV peak visible, see Fig. (15). The electron accumulation areas underneath the oxide layers effective shorten all strips and the guard ring area. The resulting high leakage current makes gamma-ray detection impossible.

For the sensors with alumina as an interstrip dielectric, we were able to distinguish the 122 keV peak from the noise for the electron and hole currents, see Fig. (16). Since the alumina acts as an effective p-stop, the leakage currents for the hole signal is low, see Fig. (17). We successfully made a DSSD on n-type material using alumina as a p-stop.

V. CONCLUSIONS AND OUTLOOK

Inter-strip shortening due to electron accumulation is a problem for any segmented p-type and double-sided n-type detectors. We showed that alumina layers can be used as effective p-stops due to a negative surface charge at the silicon-alumina interface. Furthermore, we made a DSSD on n-type silicon with alumina as the effective p-stop. We collected Co-57 gamma-ray spectra using this DSSD.

We are currently determining the exact interface charge of the alumina layer and if the charge changes under irradiation. Furthermore, we will re-design the front and back side metal layers in order to prevent the formation of high electric fields at the metal layer edges.

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REFERENCES


