Front-End ASIC for Co-Planar Grid Sensors

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Abstract—An Application Specific Integrated Circuit (ASIC) for Co-Planar Grid (CPG) sensors is presented. The ASIC provides low-noise amplification of grids and cathode signals, difference between grid signals with adjustable relative gain, shaped signals with baseline stabilization, and timing signals. In the current version the peaking time of the shaped pulses is 5μs and the gain can be switched between 36mV/fC and 18mV/fC covering an energy range up to 3MeV. Designed in CMOS 0.25µm technology it dissipates 25mW from a single +2.5V supply. A description of the ASIC and the results of its characterization with CdZnTe CPG sensors are presented. The system is analyzed in terms of resolution, and the impact of the noise correlation due to the inter-grid capacitance is discussed.

I. INTRODUCTION

The Co-Planar Grid (CPG) sensing technique has been successfully combined with recent advances in Cadmium Zinc Telluride (CZT) manufacturing, resulting in large-volume high-resolution room temperature Gamma-ray spectrometers. Due to their efficiency and compactness the CPG sensors are being considered in an increasing number of applications, ranging from nuclear material safeguard to radioisotope identification in security and defense, environmental remediation, well logging, medical diagnostics, and gamma-ray astronomy [1-4].

By subtracting the signals from two co-planar digitized grid electrodes (collecting grid and non-collecting grid) the CPG becomes sensitive to electrons only, overcoming the limit of poor holes mobility typical of the CdZnTe material. In order to compensate for the residual electron trapping, two techniques were proposed. The first consists of lowering below the unity the gain G of the non-collecting grid relative to that of the collecting grid [5]. The second consists of keeping G=1 and weighting each event by measuring its depth of interaction through simultaneous processing of grids and cathode signals [6].

The availability of a front-end Application Specific Integrated Circuit (ASIC) capable of amplifying and suitably processing the signals from CPG sensors is attractive, especially in developing portable and battery operated detection systems. The ASIC presented here serves this purpose, providing simultaneous low-noise amplification of grids, difference and cathode signals, adjustable relative gain, and timing signals.

II. ASIC ARCHITECTURE

In Fig. 1 the block diagram of the ASIC is shown. It implements three front-end channels. Two channels provide amplification and processing of the two grids signals (collecting and non-collecting). One channel provides amplification and processing of the cathode signal.

![Fig. 1. Block diagram of the ASIC.](image)

The grid electronics is composed of two low-noise charge amplifiers followed by a difference amplifier. The charge amplifiers have n-channel input MOSFETs and are based on the dual-stage charge gain circuits described in [7] where the first stage is the old configuration (Fig. 3 of [7]) with gain equal to 16 and the second stage is the new configuration (Fig. 4 of [7]) with gain adjustable to 3 or 6. Before entering the difference amplifier, each signal goes through an additional circuit, not shown in Fig. 1, generating the first pole of the shaper [7]. Three additional buffers make available the two unshaped signals (after the first pole) and their difference to dedicated outputs.

In Fig. 2 a detail of the difference amplifier is shown. The relative gain G can be adjusted through a combination of switches (S1, S2 and S3) and an external resistor Rx following the equation:

$$ G = \frac{35k}{50k} \left( 1 + \frac{50k}{35k} \right) \frac{R_1}{(20k + R_x)} $$

(1)

where Rx is the resistance seen between nodes a and b and resulting from the combination of S1 and S2.
If the switch S3 is open the relative gain G equals 1, 0.62 and 0.51 when respectively S1, S2 and S1+S2 are closed. Due to the limited matching between resistors, these values must be considered accurate within a few %. If the switch S3 is closed the relative gain G depends on Rx as shown in Fig. 3. It is also possible to disable the non-collecting channel providing an effective gain G=0. The difference signal feeds a comparator with externally controllable threshold thus generating the corresponding timing signal.

In both cases the shaping is a 5th order with complex conjugate poles [8] and band-gap referenced baseline stabilizer (BLH) [9]. In Fig. 4 the schematic of the shaping amplifier is shown. As previously discussed, the first pole is generated right after the charge amplifier circuit. The peaking time is set to 5µs.

Each channel implements a 500fF test capacitor which can be externally enabled through dedicated switch. The gain can be switched between 36mV/fC and 18mV/fC in order to cover an energy range up to 3MeV. The total dissipated power is 25mW from a single +2.5V supply. The technology is TSMC 0.25µm and the layout size (shown in Fig.5) is 3.1×3.1 mm².

III. NOISE ANALYSIS

The dual-channel electronics for the grid signals requires a dedicated noise analysis. In Fig. 6 a schematic for the evaluation of the Equivalent Noise Charge (ENC) is shown.

In Fig. 6 S_p, S_s, and S_{ig} are the power spectral densities associated to the respective noise generators. C_a and S_a are respectively the input capacitance and the noise spectrum of charge amplifier. S_p=2qI_p+4kT/R_p is related to the bulk current component I_p and bias resistor R_p of each grid. S_{ig}=\tau_3qI_{ig} is related to the inter-grid current component I_{ig}. C_g is the grid plus interconnects capacitance, and C_{ig} is the inter-grid capacitance. Q is the charge released by the sensor and, due to the nature of the CPG, can be concentrated at the input of the collecting grid.

The schematic in Fig. 6 can be easily transformed in the one in Fig. 7, where the correlation between the equivalent noise generators due to C_{ig} and S_{ig} was taken into account.
and for $G=0$ and up to channel, is not limited to operates in dual channel, when compared to the single capacitive terms. It can be observed that the increase in the results reported in [10-12], the last term was neglected.

Concerning the first approach, the r.m.s. noise on the depth of interaction, but the resolution may be different. The measurements with the internal shaper are shown. Also in this case the delay between the difference timing and the cathode ENC at shorter peaking times with sensor biased was higher than expected and needs to be investigated.

In Fig. 7 the ENC can be written:

$$\text{ENC}^2 = \left[C_T + C_g G\right]^2 + \left[C_f + C_d G\right]^2 \left[\frac{2\pi a_f A_f}{\tau_p} + S_g a_w S_a + \frac{2\pi a_w A_w}{\tau_p} + S_f \tau_p a_p\right]$$

(2)

where $S_a$ and $A/f$ are respectively the white and $1/f$ noise component of the amplifier noise spectrum $S_a$ and $a_w$, $a_f$ and $a_p$ are the coefficients related to the shaper. In the two extreme cases $G=0$ and $G=1$ it follows respectively:

$$\text{ENC}^2 = \left[C_a + C_g + C_d\right]^2 \left[\frac{2\pi a_f A_f}{\tau_p} + S_g a_w S_a + \frac{2\pi a_w A_w}{\tau_p} + S_f \tau_p a_p\right]$$

(3a)

$$\text{ENC}^2 = 2\left[C_a + C_g + 2C_d\right] \left[\frac{2\pi a_f A_f}{\tau_p} + S_g a_w S_a + \frac{2\pi a_w A_w}{\tau_p} + 2S_f \tau_p a_p\right]$$

(3b)

In (3) we assumed $C_f << C_T$, while, in agreement with the results reported in [10-12], the last term was neglected ($\alpha << 1$). Since in CPG sensors $C_g$ can be on the order of tens of pF, it may easily dominate compared to the other capacitive terms. It can be observed that the increase in the ENC component related to the series noise when the system operates in dual channel, when compared to the single channel, is not limited to $\sqrt{2}$. It can actually approach $\sqrt{2}$ for $G=0$ and up to $2\sqrt{2}$ for $G=1$. The increase in the ENC component related to the parallel noise remains $1$ for $G=0$ and $\sqrt{2}$ for $G=1$.

With regards to the second compensation method described in Section I and based on the measurement of the depth of interaction, it might be of interest a comparison between the energy ratio approach and the timing difference approach. In the first case the ratio between the cathode energy and the difference energy is measured. In the second case the delay between the difference timing and the cathode timing is measured. In both cases the result is related to the depth of interaction, but the resolution may be different. Concerning the first approach, the r.m.s. noise on the depth measurement $d$ can be approximated with:

$$\sigma_d = \frac{d_{\text{max}}}{V_d} \sqrt{\sigma_{\text{enc}}^2 + \sigma_{\text{vd}}^2 V_d}$$

(4)

where $d_{\text{max}}$ is the thickness of the sensor, $\sigma_{\text{enc}}$ and $\sigma_{\text{vd}}$ are respectively the r.m.s. noise of cathode and difference signals, and $V_c$ and $V_d$ are the amplitudes of cathode and difference signals. Concerning the second approach, by taking into account that the slope of the cathode signal, being related to the electrons traveling in the bulk, is independent of the amplitude, the r.m.s. noise in the depth measurement can be approximated with:

$$\sigma_{d_2} = \frac{d_{\text{max}}}{V_d} \sigma_{\text{vd}}$$

(5)

where the term due to the difference signal, characterized by a high slope, was neglected.

A comparison between (4) and (5), along with the ballistic deficit associated to the measurement of the cathode energy, suggest that the second approach may offer better resolution. In addition, if the timing is performed on the grid signals only (e.g. collecting and difference), the depth of interaction can be measured without information from the cathode, with consequent benefits in terms of complexity, power, and real estate.

IV. FIRST EXPERIMENTAL RESULTS

The ASIC was characterized with a $15\times15\times7$ mm$^3$ CdZnTe CPG sensor from eV-Products (II-VI Inc.). In Fig. 8(a) measurements of the ENC vs peaking time with the CPG sensor connected to the ASIC and unbiased are shown for the cathode and grid difference with $G=0$, 0.5 and 1. The measurements with the internal shaper are also shown. In our case $C_g=10$pF, $C_{ig}=14$pF, $R_g=22$M$\Omega$. The increase in ENC from $=500$e$^-$ at $G=0$ to $=900$e$^-$ at $G=1$ confirms the noise correlation discussed in previous section. The ENC of the ASIC, limited to the series noise component, can be roughly approximated with:

$$\text{ENC}_{\text{series}} = \sqrt{1 + G^2} \left[300 + \frac{7}{pF} \times [C_w + C_{ig}(1+G)]\right]$$

(6)

In Fig. 8(b) the same measurements of the ENC vs peaking time with the CPG sensor connected and biased at 1000V/80V (cathode/difference) are shown. Also in this case the measurements with the internal shaper are shown. In our case $I_{\text{le}}=6$nA was extracted, in agreement with a measured cathode leakage around 12nA at 290K, while the contribution from $I_{\text{ig}}$, measured in the range of tens of nA, was negligible, in agreement with other results [10-12]. The cathode ENC at shorter peaking times with sensor biased was higher than expected and needs to be investigated.

In Fig. 9 the measured collecting, non-collecting, difference and shaped responses to a charge $Q=27$fC injected
through test capacitors are shown for the cases $G = 0$, 0.51 and 1. An integral linearity error below $\pm 0.25\%$ for energies up to 1.5MeV (3MeV for lower gain setting) was measured.

In Figs.10 the unshaped responses of the ASIC-CPG to $^{137}$Cs signals for (a) interaction close to anode and (b) interaction close to cathode are shown. When the interaction is close to the anode, the cathode signal has low amplitude and the time delay from the interaction to the difference signal is negligible. When the interaction is close to the cathode the cathode signal has high amplitude and the time delay from the interaction to the difference signal, due to the transit time of the electrons, can be of several hundreds of nanoseconds (about 400ns in our case).

In Fig.11 the unshaped and shaped responses of the ASIC-CPG to $^{137}$Cs difference and cathode signals are shown. Anode and cathode shaped signals can be used for measurements of the depth of interaction [6].

In Fig.12 the unshaped and timing responses of the ASIC-CPG to $^{137}$Cs signals for (a) interaction close to anode and (b) interaction close to cathode are shown. Anode and cathode timing signals can be used as an alternative method for the measurement of the depth of interaction.

In Fig. 13 (a) the spectrum from a $^{137}$Cs source is shown. The spectrum was measured at $T=290K$ using the first compensation technique described in Section I [5]. A FWHM=16keV ($\approx 2.4\%$) at 662keV was measured with $G=0.86$. Fig. 13(b) shows the FWHM vs the relative gain G, measured at $T=300K$, on the 662keV peak of $^{137}$Cs and on the peak from the test pulse. It can be observed, along with a minimum for the FWHM of the 662keV peak, a trend in the FWHM from the test pulse in line with the other results. At this temperature the contribution from the bulk leakage current was about twice the one at 290K.
An ASIC for CPG sensors is being developed. Measurements adopting relative gain compensation are in agreement with the expectations. Measurements of depth of interaction from difference/cathode energy ratio and cathode-difference time delay are in progress. Noise analysis and experimental results suggest, for future optimization, the reduction of front-end noise and an adjustable peaking time. Relevant reduction in noise can be achieved by adopting a p-channel input MOSFET [13]. Additional functions like peak detectors for the shaped signals and time-to-amplitude converter for the timing difference can be implemented.

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VII. REFERENCES