DEVELOPING THE NEXT GENERATION COCKPIT DISPLAY SYSTEM

B. C. Read III, D. Barker, R. G. Bishop, L. M. Concha, J. M. Emmert, R. L. Ewing,
G. L. Fecher, P. Jarusiewic Jr., G. D. Peterson, M. Rubeiz, A. M. Sayson

US Air Force, Wright Laboratory
Solid State Electronics Directorate, WL/ELED
Wright Patterson, AFB, Ohio 45433-7511

ABSTRACT

The goal of advanced cockpit display systems is to present large amounts of information quickly and in an understandable format, enabling the aviator to improve mission performance. Wright Laboratory is developing a program to dramatically improve current display systems. Current front-line cockpit display systems utilize low-resolution analog video to present two dimensional (2-D) images on many separate displays. The future cockpit will be capable of integrating large picture digital video with three dimensional (3-D) and 2-D color images. This system will be capable of rendering icons, maps, and world-views. It will be compatible with head mounted displays and multiple large displays to improve war-planning and combat aviator situational awareness.

Wright Laboratory is developing this system in conjunction with Honeywell Technology Center. We are developing a massively parallel 3-D renderer which will be capable of updating 500,000 3-D triangles per second with shading, lighting, transparency, texture mapping, and hidden surface removal. The renderer design, based on a University of North Carolina pixel planes design, employs a massively parallel architecture with 1,024 ALUs per chip to display one million antialiased vectors per second. Current high end workstations are capable of these display goals, but fall far short of military reliability, size, and power requirements. The rendering system will be small enough to fit on one board, extensible to dual-seat configuration, and capable of up to eight windows per display channel.

1. INTRODUCTION

Today more than ever aviators are presented with a barrage of information. Victory in the air increasingly hinges on who can absorb data and utilize it effectively. Toward this end, our warfighters require the fastest and most advanced cockpit displays we can produce with current technology. At the same time, the Air Force must acknowledge limited funds and embrace ideas such as employing Commercial Off The Shelf parts (COTS). This paper outlines a program to substantially improve today’s cockpit display capabilities with a high performance and cost effective mix of COTS parts and internally researched custom components.

Current front-line fighters display two dimensional, monochromatic images on multiple displays driven by several different rendering sources and systems. The Panoramic Cockpit Control and Display System (PCCADS) 2000 study indicated that large, high resolution images can improve fighter pilots’ reaction time [1]. This is achieved by bringing the large number of disjointed displays and classic “steam gauges” into an integrated, unified display environment using standard information formats such as common colors, icons, etc. This progression is illustrated in Figure 1. The study also indicated that information presented in 3-D can convey much more information than current 2-D displays.
Table 1. Cockpit Display Comparisons [2]

<table>
<thead>
<tr>
<th>Capability</th>
<th>Last generation</th>
<th>Current generation</th>
<th>Next Generation</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-D Stroke only</td>
<td>1M vectors per sec.</td>
<td>1M anti-aliased vectors per sec</td>
<td></td>
</tr>
<tr>
<td>3-D</td>
<td>---</td>
<td>---</td>
<td>500K Polygons per sec</td>
</tr>
<tr>
<td>Color</td>
<td>---</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Sensor Video</td>
<td>Analog</td>
<td>512x512</td>
<td>1024x1280</td>
</tr>
<tr>
<td>Size</td>
<td>14 boards</td>
<td>4 boards</td>
<td>1 board</td>
</tr>
</tbody>
</table>

2. SYSTEM DESCRIPTION

Current graphics technology is capable of meeting most of the desired technical requirements with no re-design required. Graphics engines today contain the processing power needed, but fall short on the size and weight specifications. A Silicon Graphics workstation will not fit in the space available on today's fighters! To solve this, our system is centered around a very dense Multi Chip Module (MCM) which reduces size and increases speed.

The graphics processing system shown in Figure 2, is based on the CDG analysis done by Honeywell described in their final report [3]. The system is divided into four major processing areas. The first function is a Data Server which can be performed by an Intel Pentium processor. This component serves as the high level controller for the system; it accepts data from the radar, sensors, and also from world maps from the mission planning computer. The second function can be executed with four Analog Devices' SHARC chips. These act as both the Geometry Engine, performing coordinate transformations, and the Polygon Manager, doing lighting, clipping, and similar functions. The third function performs two tasks: the Tile Flow Manager, which sorts and sends the frames to the Renderer/Smart Memory and the Vertex to Planar converter which transforms the

Figure 1. Current (top) and Future (bottom) Generation Cockpits.
incoming data into the correct format for the RenderedSmart Memory.

As described above, most of the functions shown in Figure 2 can be performed with COTS chips without sacrificing latency or speed. The rendering function is the system bottleneck because it requires more processing power than is available using COTS parts. This is where our research efforts have focused. The solution we are enacting is called the Enhanced Memory Chip (EMC) and is described in the next section.

3. ENHANCED MEMORY CHIP

With current COTS chips the RenderedSmart Memory functions of the CDG system would not be capable of achieving the processing goals required in this system. In order to solve this, a custom ASIC chip (EMC) was designed. The main reason the EMC outperforms COTS chips is its exploitation of the inherently regular structure needed in pixel processing. This is done by rendering multiple pixels simultaneously with a massively parallel Single Instruction Multiple Data (SIMD) architecture. The architecture is based on the University of North Carolina's (UNC) Pixel Planes V design [4]. This architecture calls for a “Smart Memory”, meaning that the memory for each pixel has a corresponding Arithmetic Logic Unit (ALU) and multiplier. Every pixel operates from the same control lines, but they process their individual data simultaneously. The drawback of this architecture is that the number of pixels needed grows quickly as the displays become larger. With a normal screen of 1024x1280 pixels, over one million ALUs, Memory, and Multipliers are needed, resulting in over 2,000 chips in the Pixel Planes IV architecture [5]. Not only is this an unacceptable number of chips for the small space available in a cockpit, but it is also an inefficient use of resources. When a typical image is rendered, some portions of the screen are very active while others have little or no information. As a result, many of the 2,000 chips idle until the heavily loaded chips are finished.
The solution enacted by WUELED is to divide the display into smaller regions which are then rendered consecutively by the same EMC. By rendering one area at a time, the EMC will not idle if an area of the display has low activity. After all screen regions are rendered the next image can be processed. In addition to higher utilization, this adaptation allows the EMC chips to be smaller and faster. It also makes the system easily expandable; by simply adding more EMC chips higher throughput can be achieved or a larger display can be supported. The basic screen portion covered with our chip was chosen by Honeywell to be 8x8 pixels [3]. There are a total of 32 of these 8x8 blocks in the current system. The basic 8x8 block is shown in Figure 3.

Figure 3. EMC Block Diagram.

With this architecture, each of the 8x8 pixels has 64 bits of memory containing information on Z-buffering, Red, Green, and Blue color data, and Alpha shading. The memory is double buffered to allow processing of the current images' information while the last frame's data is still being written out. The 8,192 bits of data are shown in Figure 3 as the Memory block. This block can be written to or read from the ALU. The memory also is responsible for writing the final pixel information off chip.

The 64 ALUs are represented by the ALU sub-block in Figure 3. The ALU's perform all the pixel calculations and are responsible for controlling when and if the results are written to the memory. They accept data from the output of the ALUs, the memory block and from the Multiplier tree.

The final component of the design is the multiplier tree. This concept, developed by the UNC design team, greatly reduces the circuitry required in performing 64 bit serial multiplies. The original design requires 384 multiplier cells, but by implementing the multiplier tree it is reduced to 127 for an 8x8 block.

The entire EMC design was described and modeled in VHHSIC Hardware Description Language (VHDL) by in-house designers. The VHDL was simulated with realistic test vectors representing real-world data to insure the chip would perform correctly when fabricated. The same VHDL code was then synthesized to schematic format. The schematic format is a netlist of common Register Transfer Level (RTL) components that directly maps to the actual circuitry on the chips. This netlist was then automatically arranged for proper fabrication using a place and route tool. The result is a layout ready to be sent to a fabrication facility for silicon processing. This design flow is completely automated from the design description in VHDL to the final layout description. The reliance on tool automation drastically reduces the engineering cost associated with designing a new chip. This design environment allows testing at every stage of the design: the VHDL level, netlist level, and layout level. Also, by evaluating this design flow the design team at Wright Labs gains valuable experience in CAD tool use which can be applied to contracts and tool development programs.

4. SUMMARY

The Cockpit Display system described in this paper will greatly enhance the display.
capabilities of tomorrow’s fighters and meets the processing goals desired for the next generation of display systems. Improvements in cost, size, weight, and ruggedness over current commercial graphics workstations make the insertion of this technology into cockpits possible. The careful use of COTS chips in this design will result in cost savings to the Air Force and insure future growth as revisions of these commercial chips are released. The use of automated design tools and in-house design talent greatly reduces the EMC design costs. The remaining system bottlenecks were alleviated with intelligent partitioning of the image data and with the speed gained by a custom chip with massive parallelism.

REFERENCES


