RAPID AND ACCURATE TIMING SIMULATION OF RADIATION-HARDENED DIGITAL MICROELECTRONICS USING VHDL

Charles P. Brothers Jr., Capt USAF
Mark A. Mehalic, PhD, Major, USAF

Air Force Institute of Technology
Department of Electrical and Computer Engineering
Wright-Patterson AFB, Dayton, OH 45433-7765

ABSTRACT

The development of a fast, yet accurate, timing simulation capability based on VHSIC Hardware Description Language (VHDL) without the use of back annotation of timing delay information is presented. This VHDL-based timing simulator is intended, primarily, for use with radiation-hardened microelectronic circuits in simulating timing of circuit operation in pre-radiation and post-radiation (one Mrad(Si) total dose) radiation environment. Additionally, this VHDL timing simulator works well, using simplified models, for conducting timing estimates of circuit operation in cases where radiation effects are not a concern. Development of the timing models used in the VHDL timing simulator are presented. The timing models are based on a gate output drive capability being represented as an equivalent drive resistance. The loads of the driving gate and the input gates are correspondingly represented by equivalent capacitance values. The resultant gate delays are calculated from the product of the drive resistance and the combined load capacitances. The implementation of the timing models are incorporated into a VHDL library composed of logic gates, latches, and flip-flops. Simulations of circuits were run in SPICE and VHDL to assess the timing accuracy and simulation run time of the VHDL-based timing simulator versus SPICE, and results are presented. Final evaluation of the simulator included testing of a microprocessor control unit. In all cases, the VHDL-based simulation runs over two orders of magnitude quicker than the equivalent SPICE simulation. In the pre- and post-radiation environment, accuracy estimates are usually within five percent and always within 12 percent.

INTRODUCTION

The overarching goal of this research is the rapid and accurate timing simulation of radiation-hardened microelectronic circuits. The first goal is to produce radiation-inclusive models that will simulate microelectronic circuits with timing accuracy that is within 10 to 15 percent of what SPICE provides. Two issues required consideration and resolution in reaching this goal: accurately simulating microelectronic circuits in a pre-radiation environment and changes in the circuit timing performance caused by radiation effects. Additionally, the models developed in this research need to simulate at least two orders of magnitude faster than SPICE simulations.

Radiation total dose affects the operation and timing performance of microelectronic circuits [1, 2]. The effects of total dose ionizing radiation were modeled at a level of 1 Mrad(Si).

Current microelectronic circuit simulations rely on SPICE running radiation-inclusive models to simulate post-radiation parameter and performance changes [3, 4, 5]. With complex integrated circuits, SPICE simulations require large amounts of CPU time. Being able to efficiently simulate these circuits, which are constructed for applications where radiation hardness is required, becomes practical using fast microelectronic circuit simulators. Event-driven simulators such as VHDL are fast but require special models to insure timing accuracy.

The development of simple generic models providing rapid and accurate timing estimates for simulating radiation-hardened microelectronic circuits, using a VHDL-based simulator, was the core of this research effort.

MODEL DEVELOPMENT

Developing a method of simulating microelectronic circuit operation and providing accurate timing estimates required five steps to be completed. First, the sources of time delays were determined. These included the intrinsic logic-block delays, fanout-induced delays, differences in sub-circuit output rise and fall times, and delay effects of a radiation-inclusive environment. Second, models that accurately estimate the timing delays were developed. Third, the models were incorporated into VHDL-useable libraries providing a simulation environment that runs simulations faster than SPICE by two orders of magnitude or more. Fourth, simple microelectronic circuits were tested to validate the operation and accuracy of the models using the VHDL-based simulation. Finally, the VHDL-based simulator was tested and validated with larger circuits (over 2800 transistors) to demonstrate the timing accuracy and the faster performance against the baseline SPICE performance.

Defined time delay sources included: time delays due to logic gate fanout loading including rise and fall times, logic gate intrinsic time delay, and radiation environment. Defining time delay sources in three steps allowed the models to be developed in independent segments.
Model development focused on modelling the time delay sources to run in an efficient manner while being incorporated into VHDL descriptions. The modelling process was divided into several separate processes. First, logic gate input load values were determined, using SPICE, for a single CMOS transistor pair in the Texas Instruments (TI) 0.8μm SIMOX fabrication process. Second, the drive capability, modelled as a resistance, was determined. The drive resistance in combination with the load capacitance defined the fanout loading effects on timing. Third, the logic gate intrinsic time delay effects were modelled as capacitance values and, in combination with the drive resistance, defined the internal intrinsic time delay of the gate. Finally, the effects of radiation on circuit timing was modelled by adjusting the values of resistance and capacitance which define the timing characteristics of each gate.

Input loads were determined first. While the capacitance of MOSFET gates vary, depending on input voltage, an equivalent average may be determined by comparing the results of delay time measurements obtained for a state transition for both a dynamic input and a fixed capacitive load. Values for the input load capacitance were determined, by using SPICE, to measure the delay time for a logic gate to change state when connected to the input of a load gate and also when connected to a fixed-value capacitor.

Next, the pull-up and pull-down drive capability was determined. In this model development, the output pull-up and pull-down drive capability were evaluated independently, since the values of the pull-up and pull-down varied significantly (based on initial SPICE simulation of the Texas Instruments, SIMOX gate-array, inverter and NAND gates).

The drive capability is represented as an equivalent resistance parameter and is determined by measuring the logic propagation delay time for various loads connected to the output. The load capacitances are known constants that are determined beforehand. The pull-up and pull-down propagation delay times are represented by the simple equations:

\[
t_p = R_{\text{pull-up}} \sum C_i, \quad t_d = R_{\text{pull-down}} \sum C_i
\]

where:
- \(t_p\) - Total Gate Delay Time, Output Going Low-to-High
- \(t_d\) - Total Gate Delay Time, Output Going High-to-Low
- \(R_{\text{pull-up}}\) - Effective Pull-Up Drive Resistance
- \(R_{\text{pull-down}}\) - Effective Pull-Down Drive Resistance
- \(C_i\) - Capacitance of the \(i^{th}\) Load

Since pull-up and pull-down propagation delay times are considered separately, independent values for \(R_{\text{pull-up}}\) and \(R_{\text{pull-down}}\) must be developed. \(R(0)_{\text{pull-up}}\) and \(R(0)_{\text{pull-down}}\) were calculated by measuring the different pull-up and pull-down propagation delay times when a logic gate output was connected to differing numbers of inverter loads in configurations representing fanouts from zero to ten. The change in the pull-up and pull-down propagation delay time, as measured in SPICE, was compared for each of the ten different fanout loads to the calculated pull-up and pull-down propagation delay time using the equations:

\[
R(i)_{\text{pull-up}} = \frac{(\tau(1)_{\text{pull-up}} - \tau(-1)_{\text{pull-up}})}{C_i}
\]

\[
R(i)_{\text{pull-down}} = \frac{(\tau(1)_{\text{pull-down}} - \tau(-1)_{\text{pull-down}})}{C_i}
\]

where:
- \(\tau(i)_{\text{pull-up}}\) - Propagation Delay Time, Output Going Low-to-High, Fanout = \(i\)
- \(\tau(i)_{\text{pull-down}}\) - Propagation Delay Time, Output Going High-to-Low, Fanout = \(i\)
- \(C_i\) - Load Capacitance

The output resistances \(R(i)_{\text{pull-up}}\) and \(R(i)_{\text{pull-down}}\) were observed to be within three percent of being a constant value. Assuming a constant value, \(R_{\text{pull-up}}\) and \(R_{\text{pull-down}}\) were calculated using the equations:

\[
R_{\text{pull-up}} = \frac{(\tau(1)_{\text{pull-up}} - \tau(-1)_{\text{pull-up}})}{10 \times C_{\text{load}}}
\]

\[
R_{\text{pull-down}} = \frac{(\tau(1)_{\text{pull-down}} - \tau(-1)_{\text{pull-down}})}{10 \times C_{\text{load}}}
\]

The pull-up and pull-down drive resistance terms are easy to calculate once the measurement circuits are setup for each of the logic gates. The drive resistance values in conjunction with the load capacitance combine to make up two of the three terms required to model a logic gates total propagation delay time. The total delay time of a logic gate is given by the equation:

\[
t_{\text{HL}} = t_{\text{HL}} + t_{\text{HL}} + t_{\text{LU}} + t_{\text{LU}}
\]

where:
- \(t_{\text{HL}}\) - Total Gate Delay Time, Output Going Low-to-High
- \(t_{\text{LU}}\) - Total Gate Delay Time, Output Going High-to-Low
- \(t_{\text{HL}}\) - Internal Intrinsic Gate Delay Time, Output Going Low-to-High
- \(t_{\text{LU}}\) - Internal Intrinsic Gate Delay Time, Output Going High-to-Low

The last parameter determined in the pre-radiation time delay model was the intrinsic delay of the logic gate. Since each gate already has a pull-up and pull-down resistive drive capability, the intrinsic delay was represented by a capacitance value. This capacitance would be summed along with all the load capacitors and then multiplied by the pull-up or pull-down drive resistance value to determine the overall logic gate time delay as shown in the equations:

\[
t_{\text{HL}}^* = R_{\text{pull-up}} \sum C_i + C_{\text{pull-up}} + C_{\text{pull-down}}
\]

\[
t_{\text{LU}}^* = R_{\text{pull-down}} \sum C_i + C_{\text{pull-up}} + C_{\text{pull-down}}
\]

where:
- \(C_{\text{pull-up}}\) - Internal Intrinsic Pull-Up Capacitance
- \(C_{\text{pull-down}}\) - Internal Intrinsic Pull-Down Capacitance

The determination of each logic gate intrinsic delay time capacitance was accomplished by making a delay time measurement, in SPICE, of the logic gate total time delay connected to a nominal fanout load. The intrinsic delay time capacitances were determined by the equations:
The effect of radiation must be accounted for in the timing models of the logic circuits. Total ionizing dose was considered with the level being fixed at the 1 Mrad(Si) level due to limitations in the radiation-inclusive SPICE models available.

The process for determining the model variables is accomplished in a 9-step process as outlined in Figure 1. To conduct the model development process for microelectronic circuits where radiation effects are not a concern, implement the first five steps outlined in Figure 1. Once the model variables are determined, the models must be implemented in a simulator. The implementation of the models into the VHDL simulator was the next task.

1. Determine load capacitance of the inverter input transistor pair.
2. Calculate pull-up drive resistance.
3. Calculate pull-down drive resistance.
4. Calculate intrinsic time delay pull-up load capacitance.
5. Calculate intrinsic time delay pull-down load capacitance.
6. Calculate post-rad total dose pull-up drive resistance.
7. Calculate post-rad total dose pull-down drive resistance.
8. Calculate post-rad total dose intrinsic time delay pull-up load capacitance.
9. Calculate post-rad total dose intrinsic time delay pull-down load capacitance.

Figure 1. Model Variable Computation Process.

LIBRARY DEVELOPMENT

VHDL code development focused on efficient implementation of the timing models describing the timing characteristics of each logic gate. VHDL descriptions were developed for each gate modelled in the TI SIMOX SPICE library. Each description contained the code necessary to simulate the function and timing performance of the logic gate. After each description was developed, it was tested against data obtained using SPICE.

All logic gates contain resistance and capacitance parameters used in determining the time delay of the gate, as shown in Figure 2. The inputs of each logic gate contains load resistance parameter values that represent the equivalent load of the gate. The load resistance, at the input of the logic gate, represents gate leakage if measurable. The capacitance at the gate input represents the input MOS gate capacitance used in determining the load seen by the driving logic gate.

The drive resistance value shown in Figure 2 represents the drive pull-up capability of the logic gate. The capacitance at the output of the gate is used to model, in conjunction with the pull-up drive resistance, the logic gate intrinsic low-to-high time delay.

The pull-up drive resistance value is modified by the radiation-inclusive models to account for exposure to radiation and compensate for changes in drive capability after exposure to radiation. The capacitance at the output of the logic gate is adjusted after exposure to radiation to account for changes in the logic gates intrinsic time. The model variables are incorporated into the logic gates in the form of generic declarations at the beginning of the VHDL code for each logic gate. The VHDL pseudo-code describing the operation of the 2-input NAND gate is contained in Figure 3.

An important part implementing the timing models into VHDL is the WIRE cell. The WIRE cell back-propagates the effective resistive and capacitive load information to the driving gate when the fanout is greater than one. The WIRE cell sums the parallel resistances and capacitances and feeds the equivalent load resistance and capacitance to the driving gate, as shown in Figure 4, where $C_e$ and $R_{en}$ are defined by the equations:

$$C_e = C_{d} + C_{p} + C_{l1} + C_{l2}$$

$$R_{en} = \frac{1}{\frac{1}{R_{p}} + \frac{1}{R_{l1}} + \frac{1}{R_{l2}}}$$

The WIRE cell can also be used when the fanout is equal to one. This allows the designer to insert wire capacitance for large wires when this becomes a factor in the circuit performance. The algorithm describing the operation of the WIRE cell is outlined in Figure 5.

SIMULATION PROCESS

Data to develop the models was recorded from SPICE signal timing data. All SPICE data was collected directly using the measure function available in HSPICE, version H92b [6]. Simulator run time data was collected directly from the simulation run time log file. Simulation of the models in VHDL was accomplished for both the base and radiation-inclusive model with the Synopsys.
VHDL Debugger, version 3.0b, using the Waveform Viewer program to manually record timing data into ASCII data files [7]. VHDL run time information was collected using a stopwatch since the simulations were run within a Synopsys graphical interface program, preventing easy access to the computer system run time collection utilities.

The choice of running the SPICE simulations using HSPICE and VHDL simulations using the Synopsys VHDL Debugger was intentional. HSPICE compiles the SPICE deck and runs the simulations using compiled computer code. The Synopsys VHDL Debugger, using the Waveform Viewer program, runs VHDL descriptions in an interpreted mode. The advantage of this choice is SPICE, the CPU intensive simulator, was running efficiently using compiled computer code while the "fast" event driven simulator, VHDL, was running in a "slower" interpreted mode. Thus, the reported run time speed-up values are conservative and even better simulation speed-up ratios should be possible.

Figure 3. Two-Input NAND Gate Algorithm.

Figure 4. Equivalent Load Schematic For Delay Time Calculation.

Three simulations are run, SPICE, radiation-inclusive model VHDL, and standard model VHDL. SPICE provides the timing performance baseline since the data obtained from SPICE is accurate and traceable to physically constructed microelectronic circuits at Texas Instruments [5]. The radiation-inclusive model VHDL is the test simulation and all of the measurements recorded are compared against the measurement values obtained using SPICE. Finally, standard model VHDL simulations are run to provide a comparison of the capability of the standard model VHDL against the results obtained using the radiation-inclusive VHDL model, both for timing accuracy and simulation run time. While functional operation should be the same for both the standard and radiation-inclusive model VHDL simulations, functional operation of both models was also verified.

Figure 5. Wire Cell Algorithm.

Data was collected for each circuit tested, confirming the functional operation, logic propagation delay timing information, and simulation run time for the various logic gates as simulated by each of the simulators.
Finally, the radiation-inclusive model VHDL descriptions can be simplified for implementation as a non-radiation environment timing simulator. The radiation-inclusive VHDL models, after simplification to remove the radiation parameter information, includes the structure necessary to provide accurate timing estimates. The method of calculating time delays, using drive resistance, load capacitance, and intrinsic internal delay time capacitance, all remain the same. The radiation-inclusive parameter variables and the radiation effects procedure calls are removed from the generic declarations of the VHDL descriptions, simplifying the descriptions. Simplifying the radiation-inclusive VHDL model descriptions allows designers to adapt the models for use in circuit design when radiation effects are not a concern, while retaining the timing accuracy of the radiation-inclusive VHDL models. Simulation run time are faster than the radiation-inclusive VHDL models but slower than base VHDL.

TEST CIRCUITS

Microelectronic circuits were selected to implement the testing goals. The specific selection of the microelectronic circuits required balancing the goals of obtaining valid test data indicating the timing accuracy against the necessary simulation run time. Every logic gate and memory circuit was tested for functional as well as timing accuracy, at the gate level, in VHDL after the models were implemented.

In addition to the tests conducted for each logic gate, a total of four circuits were selected and simulated. A four-bit adder represented the least complex circuit and has the lowest total transistor count of the four circuits. The other three circuits tested included, a binary coded decimal (BCD) to seven-segment converter, microwave oven controller, and 16-bit microprocessor control unit.

The ripple-carry four-bit adder was selected because a chain of four full-adders is sufficient to test the VHDL library, complete with the three logic gates and the WIRE cell. The WIRE cell was used at two different levels and connected to other WIRE cells insuring that the full function of the cell was tested.

The second logic circuit chosen was a BCD to seven-segment converter. This implementation of the converter was not intended to be the fastest or the smallest implementation of the circuit. Instead, this circuit was designed to use several of the logic gates implemented in radiation-inclusive model VHDL library, which were not used in the four-bit adder circuit, while providing reasonable size and timing performance.

The converter gate count is slightly lower than the four-bit adder gate count, with a total gate count of 37, for the BCD to seven-segment converter. However, there was no repetition of sub-circuits in the BCD to seven-segment converter, while the adder is constructed of four repeated full-adder blocks. Additionally, the BCD to seven segment converter has a higher total transistor count; 222 transistors versus 184 transistors in the four-bit full-adder circuit.

The first two circuits contained exclusively combinational logic gates. The third circuit, a state machine control unit, in the form of microwave oven control unit, was selected because it contained two types of state memory cells, the D flip-flop and D latch. Additionally, this circuit incorporated a tri-state output inverter to allow disconnection of the output drive signals. The circuit designed was a simple state machine to control the operation of a microwave oven. It was designed by writing a behavioral VHDL description and then synthesizing a structural circuit using the Synopsys Design Analyzer, version 3.0b [8]. The circuit, as designed, contains 446 transistors organized into 67 gates.

The final circuit, a 16-bit microprocessor control unit, was selected to provide a more complex circuit containing a much larger number of logic gates than the previous three circuits. The large number of logic gates, in different combinations, allowed testing to confirm the flexibility and accuracy of the radiation-inclusive VHDL model. Simulation run time versus logic gate count verified the efficiency in scaling of the radiation-inclusive VHDL model simulator runs versus SPICE.

The 16-bit microprocessor control unit chosen was designed using a state timing table developed as part of a class project [9]. For this research, the state timing table was synthesized into structural VHDL using the Synopsys Design Analyzer. The structural VHDL was simulated for function and the results agreed with the data presented in the class project report.

The 16-bit microprocessor control unit, as implemented, is constructed of 536 logic gates and incorporates 61 WIRE cells. The 536 logic gates use 2864 transistors, representing a circuit containing roughly one order of magnitude more circuit elements than the previous circuits tested for this research.

Signals were selected for monitoring the various state propagation delay times for various outputs of the control unit. The large circuit size limited the input stimulus that could be tested in a reasonable amount of time. For the purpose of this research, it was reasonable to select several output signals that are timed off of the clock signal driving the D flip-flops. SPICE simulation of the microprocessor power-up reset cycle, representing the first 400 ns of operation, requires several hours of simulation time for a single pass running on a Sun Microsystems SPARCstation II computer system.

Simulation of timing accuracy was accomplished by first selecting an input-to-output signal data set for each microelectronic circuit. The input signals were then programmed as stimuli for each simulator run. Second, each circuit was simulated in SPICE and in the radiation-inclusive model VHDL for several different radiation environments. Third, all the circuits were simulated using the base VHDL in the pre-radiation environment. Output signal time delay information was collected during or after each of the simulator runs.

The base VHDL, used in the comparisons for this research, used the same functional descriptions as the radiation-inclusive model VHDL. The only difference between the two VHDL simulations was the method of calculating the time delay information for each gate. While the radiation-inclusive model VHDL used the load values in calculating the time delay through each gate, the base VHDL used a constant load value for the delay time calculation. The base VHDL gate descriptions were constructed with conventional time delay values for the logic transitions.

Data presented on the timing accuracy of the radiation-inclusive model VHDL and the standard model VHDL were compared directly with the results obtained using SPICE. The timing errors were recorded in percentages and the SPICE value was used as the reference value for the calculations.
SIMULATION RESULTS

The overall results of simulating each circuit was presented, showing the run time and timing errors observed for base-VHDL, radiation-inclusive model VHDL, and SPICE simulations for each of the four circuits. The mean of the absolute value of the error (μ) for each logic signal state transition time delay was calculated using the equation:

\[ \mu = \frac{1}{n} \sum_{i=1}^{n} |(\Delta t_{i\text{VHDL}} - \Delta t_{i\text{SPICE}})| \]  

where:
- \( n \) - Number of Signal Transitions Measured in Each Circuit
- \( \Delta t_{i\text{VHDL}} \) - VHDL Time Delay of the \( i \) Signal Transition
- \( \Delta t_{i\text{SPICE}} \) - SPICE Time Delay of the \( i \) Signal Transition

The standard deviation (σ) of the timing error absolute values was also calculated for each circuit using the equation:

\[ \sigma = \sqrt{\frac{1}{(n-1)} \sum_{i=1}^{n} [(\Delta t_{i\text{VHDL}} - \Delta t_{i\text{SPICE}}) - \mu]^2} \]  

After the calculations were accomplished for a given circuit, the results were plotted on showing the relative run time versus timing accuracy performance for each simulator. An ideal simulator would have both a zero percent timing error and zero run time.

Results are shown for each of the four circuits simulated. The run time versus timing error is shown for both the pre-radiation and 1 Mrad(Si) total dose radiation-inclusive VHDL model.

The values for μ are 2.3 percent and 2.5 percent respectively. The error bars show σ for μ of the timing error. The σ values for pre- and post-radiation-inclusive model VHDL simulation runs are 1.6 percent and 1.7 percent respectively. The base VHDL simulator run timing error, μ was 29.7 percent and σ was 19.4 percent.

Simulation of the radiation-inclusive VHDL model, four-bit adder demonstrated a dramatic improvement in timing accuracy calculation over the base-VHDL results, but with a run time penalty. The radiation-inclusive model VHDL ran two to three times slower than the base-VHDL. The initial results of testing the timing models, incorporated into VHDL descriptions and simulated as a four-bit full-adder, indicated the timing models would meet the indicated goals of simulating a circuit two orders of magnitude faster while retaining timing accuracy to within ten to 15 percent of the results obtained using SPICE. Because the four-bit adder contained only three different logic gates, additional testing was required with more complex circuits.

The second combinational logic circuit tested was the BCD to seven-segment converter circuit. This circuit is a more diverse and complex circuit than the four-bit full-adder. Testing the radiation-inclusive model VHDL simulator required additional data collection to accurately characterize timing accuracy. A total of 24 different time delay signal transitions were recorded.

The summary results of the time delay error measurements are shown in Figure 7. The simulation run times for each simulator were considerably longer than the run times observed for the adder circuit. Each SPICE simulation took an average of 940 seconds to run, radiation-inclusive VHDL simulation took 1.9 seconds to run, and base-VHDL simulation ran in 1.1 seconds. The μ for the pre-radiation VHDL simulation was 4.1 percent while μ for the post-radiation was 3.8 percent. The σ for the pre- and post-radiation VHDL data was 2.7 and 2.8 percent respectively.

Timing error and standard deviation were calculated using Equations (8) and (9). The timing error results for the 18 different time delay signals of the four-bit full-adder are shown in Figure 6. Each simulator run time is represented using a logarithmic scale on the x-axis, while the timing accuracy error is shown using a linear scale on the y-axis. All simulation run times shown for the base VHDL, radiation-inclusive model VHDL, and SPICE are the average run time for a single simulation. Both the pre-radiation and 1 Mrad(Si) total dose results are shown for the radiation-inclusive VHDL model.

The microwave oven controller circuit added two different state machine devices and the tri-state inverter to the testing, the first complex circuit tested with state machine logic devices. The
radiation-inclusive model VHDL simulator timing error and standard deviation were calculated using Equations (8) and (9).

Figure 8. Microwave Oven Controller, Simulation Timing Errors.

The $\mu$ and $\sigma$ of the time delay error measurements are shown in Figure 8. The simulation run times for each simulator were considerably longer than the run times observed for either of the previous circuits because of the circuits complexity. Each SPICE simulation pass took 10,800 seconds to run; radiation-inclusive VHDL simulation took 5 seconds to run; and each base-VHDL simulation ran in 1.8 seconds. The $\mu$ for the pre-radiation VHDL simulation was 3.0 percent while the $\mu$ for the post-radiation was 3.2 percent. The $\sigma$ for the pre- and post-radiation VHDL data was 3.0 and 2.9 percent respectively.

The base-VHDL error results are shown in Figure 8, at 1.8 seconds run time. The $\mu$ for the base-VHDL simulation run was 13.5 percent with a $\sigma$ of 7.2 percent.

The final and most complex circuit tested in this research effort was a 16-bit microprocessor control unit. The radiation-inclusive model VHDL simulator timing error and standard deviation were calculated using the same method as the previous three circuits.

Figure 9. 16-Bit Microprocessor Control Unit, Simulation Timing Errors.

The $\mu$ and $\sigma$ of the time delay error measurements are shown in Figure 9. The simulation run times for each simulator were far longer than the run times observed for any of the previous circuits. Each SPICE simulation pass took an average of 210,000 seconds (55 hours) to run; radiation-inclusive VHDL simulation took 32 seconds; and each base-VHDL simulation ran in 15 seconds. The $\mu$ for the pre-radiation VHDL simulation was 2.4 percent while the $\mu$ for the post-radiation was 2.3 percent. The $\sigma$ for the pre- and post-radiation VHDL data were both 1.5 percent.

The base-VHDL error results are shown in Figure 9, at 15 seconds run time. The $\mu$ for the base-VHDL simulation run was 17.6 percent with a $\sigma$ of 11.4 percent.

Timing accuracy for the radiation-inclusive model VHDL simulating the 16-bit microprocessor agreed well with the SPICE simulation results, with the mean error being under 3 percent. Although the most complex circuit tested, similar timing accuracy results were obtained from the radiation-inclusive model VHDL simulations as were obtained with the first three circuits tested.

As the circuits increased in complexity, the ratio of the VHDL to SPICE run times increased significantly. In the four-bit full-adder, the run time ratio of the SPICE to the radiation-inclusive model VHDL simulations was over 380 to 1. In the final circuit tested, the 16-bit microprocessor, the ratio of the run times of SPICE to the radiation-inclusive model VHDL simulations was over 6000 to 1. This increase in the run time ratio was due to the VHDL being an event driven simulator, while SPICE is a node driven simulator. The difference in run time between the two different VHDL simulators was due to the increased complexity incurred in calculating each logic gate transition time delay for the radiation-inclusive model VHDL simulations.

Timing accuracy of the radiation-inclusive model VHDL remains consistent over all four of the circuits tested, with the mean error remaining under 4.5 percent for all four circuits. Timing accuracy of the base-VHDL varied greatly, depending on individual signal paths. Since the time delay for each logic gate in the base-VHDL was fixed, any variance in fanout loading led to large errors in the time delay estimates. While the radiation-inclusive model VHDL required more CPU time to simulate than the base-VHDL, it was orders of magnitude faster than SPICE. The radiation-inclusive model VHDL provided timing estimates that were within a few percent of the values obtained from SPICE.

ERROR SOURCES

The identified sources of error include: multiple pull-up and pull-down, rise and fall rate variation, model variable units, and SPICE run-to-run variability. The largest observed error source is multiple pull-up and pull-down. Another significant source of error, is differences in logic gate rise and fall rates. Smaller error sources were identified that were due to limits imposed by the base units, capacitance and resistance, chosen for the time delay calculations. SPICE simulations were not perfectly repeatable, leading to errors in modeling the logic gate time delays.

The phenomena causing the largest observed timing error, ten to 11 percent, was due multiple pull-up and pull-down induced timing errors. The three-input NOR gate has the potential for the pull-up drive capability to be as large as three single pull-up outputs. The three-input NAND gate has the potential for the pull-down drive capability to be equivalent to three single pull-down outputs. The increased drive capability shortens the actual time delays significantly, while the radiation-inclusive VHDL models do not.
model the faster delay times. The only provision for a multiple pull-up or pull-down timing change is a Glitch report is issued, as indicated in Figure 3.

To improve the radiation-inclusive model VHDL timing accuracy, multiple pull-up and pull-down timing effects must be determined, which will decrease the logic-gate state-transition time accuracy, multiple pull-up and pull-down timing effects must be indicated in Figure 3.

time of the gates in the succeeding stage. In this research effort, an attempt was made to account for differing rise and fall times by measuring transition delay time after an inverter in the succeeding stage. This method of rise and fall time compensation used in the radiation-inclusive model VHDL worked better than no rise and fall time compensation and provided over a five-percent improvement in the no rise and fall time compensation timing estimates, as tested in the single logic gate tests.

Changing the base units of the capacitance parameter would increase the accuracy of timing delay calculations. The base capacitance unit chosen for this research effort was the femtofarad, but after data collection, it became apparent that a smaller base unit would increase accuracy in intrinsic time delay estimates. Round off, in the worst-case condition, led to timing estimate errors slightly greater than one percent.

Results of the circuit simulation runs of SPICE were not identical when the transistor net list order was changed. SPICE is a node driven simulator which generates variations in the results caused by the node variables varying in value when stored in the computer running the simulation. Differences in the simulation variable magnitudes being used to calculate node voltage and current values for each time slice has an effect on simulation accuracy. Delta time errors also occur as the time slices are shortened in an attempt to simulate circuit operation more accurately. In some cases tested, input-to-output transition time delays varied by as much as one percent when the SPICE node matrix was reordered. Since SPICE simulation results varied, VHDL timing models developed could not be expected to yield better results than the SPICE data provided.

CONCLUSION

The radiation-inclusive model VHDL-based simulator is an accurate timing simulator with the absolute value of the mean error (µ) remained under 4.5 percent for all circuits tested. The pre-radiation values of µ for the four-bit adder, BCD to seven-segment converter, microwave oven controller, and 16-bit microprocessor control unit were 2.3, 4.1, 3.0, and 2.4 percent respectively.

The radiation-inclusive VHDL model is able to simulate VLSI circuits efficiently with the simulation run time ratio improving over SPICE as the circuit becomes more complex. The simulation run time ratio for the four-bit full-adder was over 380 times faster for the radiation-inclusive VHDL model than SPICE. The simulation run time ratios for the BCD to seven-segment converter and the microwave oven controller were 500 and 2100 respectively. Likewise, the simulation run time for the complex 16-bit microprocessor control unit was over 6000 times faster than SPICE with no degradation in timing accuracy.

Three areas of the timing estimation modeling have been identified as needing additional modifications to improve the accuracy of the VHDL-based timing simulator. First, significant errors were observed in the modeling of multiple pull-up and pull-down input to output transitions. Second, variability in rise and fall times affected logic transition of downstream gates. Third, the resistance and capacitive units used to calculate output transition changes of gates are defined in terms of physical units with base units of the ohm and femtofarad.

This research effort demonstrated that it is possible to simulate microelectronic circuits orders of magnitude faster than SPICE while still maintaining reasonable accuracy. Timing accuracy is maintained for the pre-radiation and 1 Mrad(Si) total dose radiation environments. Additional modifications to the radiation-inclusive models could enable increases in timing accuracy without substantial simulation run time penalties.

REFERENCES