DESIGN ENHANCEMENTS FOR THE AIR FORCE INSTITUTE OF TECHNOLOGY'S WINOGRAD FOURIER TRANSFORM PROCESSOR

Raymond E. Sommer and Mark A. Mehalic

Department of Electrical and Computer Engineering
Air Force Institute of Technology
Wright-Patterson Air Force Base, Ohio 45433

ABSTRACT

The Air Force Institute of Technology (AFIT) is currently developing a Winograd Fourier Transform Processor made up of three Winograd Fourier Transform Algorithm (WFTA) chips developed at AFIT. The processor can be hardware configured to perform a 15-, 16-, 17-, 240-, 255-, 272-, or 4,080-point transform. This paper presents three methods that can be used to improve the utility of the AFIT WFTA processor. Dynamic reconfiguration, a two-dimensional transform system, and an alternate architecture for the AFIT WFTA are presented. Results of these improvements are given, including a four-dimensional FFT configuration that can perform a single 77,520-point complex FFT in 8.87 milliseconds, and once the processors pipeline is full, a 77,520-point complex transform would be completed every 2.22 milliseconds.

INTRODUCTION

In many areas of digital signal processing, there arises the need to efficiently compute the Discrete Fourier Transform (DFT). In an effort to satisfy this need, the Air Force Institute of Technology (AFIT) is developing a Winograd Fourier Transform Processor made up of three Winograd Fourier Transform Algorithm (WFTA) chips designed at AFIT. The three chips, a 15-, 16-, and 17-point WFTA, are combined using the Good-Thomas Prime Factor Algorithm to perform up to a 4,080-point complex transform. The overall design of the AFIT WFTA processor requires the three WFTA chips (performing the transforms), a Prime Factor Algorithm (PFA) chip (to control the operation of the processor), and four dual-port memory chips (used to hold data at intermediate stages). The 4080-point configuration is shown in Figure 1. The processor can be hardware configured to perform a 15-, 16-, 17-, 240-, 255-, 272-, or 4,080-point transform [1].

Several areas can be addressed to improve the utility of the WFTA processor. First, the WFTA processor can be given the ability to dynamically reconfigure the processor for the seven transform sizes. Second, methods to generate larger transform sizes with the WFTA processor could be developed. Finally, changes to the WFTA architecture can be attempted to expand the WFTA's overall utility.

This paper presents three methods that can be used to improve the AFIT WFTA processor. First, two data path configuration schemes are introduced that allow dynamic reconfiguration of the WFTA processor. Second, the use of the AFIT WFTA processor to perform transforms on one dimension of a two-dimensional transform system is investigated. The choice of the second dimension's processor is discussed along with problems that arise with such an implementation. Finally, an alternate architecture for the AFIT WFTA is suggested. This new architecture results in a processor chip set that is easier to test, more robust, allows automated address chip generation, allows four-dimensional FFTs, and enables the processor chip set to expand.

Dynamic Transform Size

The current WFTA architecture supports the transform sizes listed above. A limitation of the current architecture is that hardware reconfiguration is required to switch between transform sizes. To make a WFTA processor more useful, the ability to dynamically configure the transform size can be
incorporated. The WFTA chips are already able to
electronic switch via the WFTA size inputs to each
chip. The data paths necessary to set up the various
transform sizes are what is missing from the current
WFTA architecture. Two solutions are proposed to
solve the dynamic configuration problem. The first
solution applies to chip-level WFTA implementations
and the second solution applies to a wafer-scale
implementation.

The chip-level solution is realized through the
use of additional memory chips as shown in Figure 2.
The memory chips would be enabled and disabled by
a three bit WFTA size vector. Depending on the
transform size selected, the necessary memory chips
would be enabled, thus setting up the required data
path. The PFA controller chip and WFTA chips would
then perform the transform. For example, to perform
a 255-point transform, memories C, H, and F would
be enabled. This places the 15- and 17-point WFTA
chips in the data path. This solution requires an
extra five memory chips and a three bit transform
size vector be generated by a modified PFA controller.

The wafer-scale solution uses multiple buses
placed on a support wafer along with a network of
T-gates used to configure the data path. Figure 3
shows how this would be implemented. Each T-gate
shown in Figure 3 represents a bank of 48 T-gates
enabled by the same control signal. As an example,
a 272-point transform would require the A, G, and F
control signals set high and the rest held low. This
configures a data path that contains the 16- and
17-point WFTA chips in the data path. This solution requires an
extra five memory chips and a three bit transform
size vector be generated by a modified PFA controller.

Both methods presented above result in a
dynamically configurable WFTA processor. The choice
of which method to use is determined strictly by the
manner by which the processor is realized: wafer-scale
or chip-level integration.

Larger Size Transforms

The WFTA processor provides seven different
transform sizes that can be applied to various DFT
problems. Methods that allow the WFTA to be used
for other transform sizes and specifically use the
WFTA to perform larger transform sizes were
reviewed. One method that appears to have promise
is using the WFTA processor to perform DFTs on one
dimension of a two-dimensional transform.

Determining what type of processor should be used to
perform the transform on the other dimension and
how to map the two-dimensional transform back into
one dimension need to be determined.

Using another WFTA transform for the other
dimension’s processor is possible as long as the other
WFTA’s transform size is mutually exclusive with the
4080-point transform of the AFIT WFTA processor [2].
Possible other WFTA transform sizes include the 7-,
11-, and 13-point transforms. Determining the
two-dimensional data mapping for the WFTA would
be difficult, but large transforms would be possible
with such a system. A more practical method of
implementing the multiple WFTA processor system is
covered in the next section.

Using a small-radix Cooley-Tukey transform is
possible if the resulting transform is a power of the
radix. For a radix-2 transform, the other transform
must be a size that can be expressed as

\[
\text{size} = 2^{(m-1)}
\]

where m is a positive integer [2]. The 16-point
WFTA would be implemented directly and other size
transforms may be possible by data-padding the WFTA
output data sets up to the next power of 2. A radix-4
transform would be implemented in the same manner.

The mapping of the input data for all of the
above solutions would be complex at best. While
these solutions may be possible, the complexity of the
solutions might preclude their implementation.
Further research must be completed before any of
these methods are pursued.

A Revised WFTA Architecture

The current AFIT WFTA chip set has the three
transform chips (15-, 16-, and 17-point) that can be
used alone or in combination with the other chips in
the set. Each of these chips has an address section
(used to generate the addresses for the input and
output data) and an arithmetic section (used to
perform the actual transform). Unfortunately, it is
not possible to use these chips directly with transform
chips other than those currently in the AFIT WFTA
chip set. This is due to the fact that the address
section of the chips contain addresses only for the
transforms that can be performed by the three AFIT
WFTA chips.
The arithmetic and address sections of the WFTA chips work in concert to perform a transform, but operate independently and perform different but related functions. Only the clocks, the Operate signal, and the DONE signal are common to the two sections. The proposed change to the WFTA architecture involves separating the current WFTA chip design into two separate chips, the WFTA arithmetic and WFTA address chips.

The new WFTA arithmetic chips would be approximately 30 percent smaller and would require only 118 pins. The new WFTA arithmetic chip would be easier to test and to verify proper operation since the arithmetic circuits would be isolated from the address circuits. Figure 5 shows the basic structure of the WFTA arithmetic chip and gives a breakdown of the required chip interface pads. The WFTA arithmetic chip would contain the arithmetic circuits, arithmetic control circuits, and test circuits for the arithmetic circuitry.

The WFTA address chip would contain the address control circuits, the WFTA address memory (XROM), the XROM address generator (x-addr-gen), and test circuits for the address chip. The address chips for all WFTA chips would be similar, differing only in the programming of the XROM and the x-addr-gen circuit. Each WFTA address chip could be packaged in a 40-pin package. Figure 6 shows the basic structure of the WFTA address chip.

By placing WFTA address and arithmetic sections on separate chips, the WFTA arithmetic chips would become more generic and could then be used with a wider variety of WFTA chips. Additional WFTA chips could be designed to expand the AFIT WFTA chip set, from which a large variety of transform sizes could be derived. For example, in addition to the 15-, 16-, and 17-point chips currently designed, 11-, 13-, 19-, and 23-point WFTA transform chips could be made. The user could then select chips from the WFTA chip set that could perform the transforms desired. Table 1 shows the large number of transform sizes that would be available if the chip set were expanded.

Once chips were selected from the WFTA chip set, a specific address set for the selected chips would have to be generated. This address set would be used to generate the XROM and other address circuitry for the address chip. The address chips could be specially fabricated for each application, or a generic address chip could be developed with a programming capability, such as laser-programmable circuits.

Placing the arithmetic and address section on separate chips has many advantages. First, the WFTA arithmetic and WFTA address chips could be developed and tested independently from each other. This would eliminate some of the problems generated by the interaction of these circuits.

Second, because the address section would be on its own chip, there would be more area available for address storage. This could allow four-dimensional WFTA transforms that could perform even larger transforms with the same data throughput available with the current AFIT WFTA. For example, operating at 70 MHz, a four-dimensional transform using 15-, 16-, 17-, and 19-point WFTA chips could be configured to perform a single 77,520-point transform in approximately 8.869 milliseconds. Once the processor's pipeline is full, a 77,520-point transform would be completed every 2.217 milliseconds.

Third, the address circuitry for all the WFTA address chips would be similar in layout and design. Software programs already exist to generate the WFTA addresses list and lay out the XROM. With minimal effort, an address chip compiler program could be derived that could completely lay out the entire address chip. The inputs to the address chip compiler would be the addresses list and the amount of delay in the arithmetic chip it would support.

The final advantage relates to the triple-redundant design described by Taylor [3]. Taylor's design has three WFTA chips performing each transform. One chip is designated as the primary data chip and the other two are watchdog chips that check the results of the primary chip. In this design, if a failure in an arithmetic circuit of one of the chips occurs, one third of the redundancy is eliminated. If the address and arithmetic sections are placed on separate chips, the triple redundant system would be as in Figure 7. If a failure in an arithmetic circuit of one of the chips occurs, only the arithmetic chip redundancy would be reduced with no loss of redundancy in the address chips. Therefore, with the same level of redundancy there is an increase in the overall reliability of the design.

The only problem associated with placing the arithmetic and address sections on separate chips is ensuring shared timing and control signals get distributed with the proper timing. The only shared signals are the 2 clocks, the Operate signal, and the DONE signal. The clocks and the Operate signal lines to the two separate chips would have to be carefully designed to ensure the signal propagation times would be the same to the input pins of both chips. The DONE signal timing is not critical.

The separation of the address section from the arithmetic section results in a design that is easier to test, more versatile, easier to implement, and more robust. The only difficulty with the design is that the shared signals must be carefully distributed to both chips.
SUMMARY

Methods have been described that would increase the usefulness of the AFIT WFTA processor. The dynamic reconfiguration of the AFIT WFTA would allow a single WFTA processor to be used to perform all of the transform sizes achievable by the AFIT WFTA chip set. Using the AFIT WFTA processor to perform transforms on one dimension of a two-dimensional transform system would increase both the number and size of transforms supported by the AFIT WFTA. Finally, changing the architecture to place the address and arithmetic functions on separate chips would open up the AFIT WFTA architecture to larger and more varied transform sizes. All of the proposed improvements to the AFIT WFTA would allow the AFIT WFTA Processor to address a wider variety of DFT problems.

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REFERENCES


Figure 1. Basic WFTA Architecture [1]
Figure 2. Reconfigurable Chip-Level Design [1]

Figure 3. Reconfigurable Wafer-Scale Design [1]
Figure 4. WFTA/Radix-2 Two-Dimensional Processor [1]

Figure 5. WFTA Arithmetic Chip Layout [1]
40-Pin Chip

13 IN ADDRESSES
13 OUT ADDRESSES
2 Vdd
2 Ground
2 CLOCKS
1 Operate
1 Test
1 DONE
1 WDenable
2 Transform size
1 WD error out

Figure 6. WFTA Address Chip Layout [1]

Figure 7. Revised WFTA Watchdog Design [1]
### Transform Sizes Available

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Table 1. Revised WFTA Architecture Transform Sizes [1]