An 8-Element 2–16 GHz Phased Array Receiver with Reconfigurable Number of Beams in SiGe BiCMOS

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Abstract — This paper presents an 8-element 2–16 GHz phased array receiver chip in SiGe BiCMOS with reconfigurable number of beams. An 8-input single-output, or a 4-input dual-output, or a 2-input 4-output beams can be synthesized in this chip. Additionally, two digital beamforming channels can also be used in this chip. The measured 2-input 4-output beam mode results in a gain of 10-11.5 dB at 2-16 GHz with excellent gain flatness. The measured noise figure and input referred $P_{1dB}$ is 11.5-12 dB and $-15±1$ dBm respectively, at 2-14 GHz. The wideband channel has a 5+3 bit phase shifter control and a 3-bit VGA ensuring a 5-bit phase response with 8 dB gain control over the entire band. The chip consumes 265 mW/channel from a 2.5 V supply.

Index Terms — Multiple-beam, phased array, phase shifter, SiGe BiCMOS.

I. INTRODUCTION

SiGe and CMOS technology which is now extensively employed for RF and digital beamforming phased-array systems results in a high level of integration between the analog RF and digital control functions (SPI), allows the integration of a large number of channels (4-16 channels) on the same chip, and in some cases, results in 2-4 simultaneous beams synthesized on-chip using RF combining techniques [1-5]. These chips are individually designed and fabricated for every specific frequency and number of beams, which results in a relatively limited number of chips for a particular application. Since the NRE (non-recurrent engineering) design and mask cost of these chips is very high, this results in a relatively high cost per chip and therefore, still limits the use of SiGe for a variety of low-cost systems.

A high-volume demand for a single-chip design can only exist when the SiGe or CMOS design satisfies multiple application needs in the same chip, such as 2-16 GHz operation (so that the chip can be used at different frequencies with nearly equal performance), capabilities of forming single or multiple beams (1, 2 or 4 simultaneous beams), capability of having a digital beamforming circuitry for sub-array beamforming, and reasonable noise and linearity performance.

This paper presents a 2-16 GHz SiGe BiCMOS 8-element phased array receiver with reconfigurable number of beams, and with digital beamforming capabilities (Fig. 1). The proposed architecture is capable of operation at any frequency and bandwidth between 2 GHz and 16 GHz with good linearity (input $P_{1dB}$=14 to -16 dBm) and noise figure (NF = 11.5-12 dB). Note that an external LNA is employed and this will determine the total system NF. The chip can be configured for 1, 2, or 4 simultaneous beams, and with added digital-beamforming (DBF) and IF down-conversion capabilities. The multiple-beam configurations can be switched electronically within the same chip and all the receiver parameters can be set using a standard serial peripheral interface (SPI).

Fig. 1. The 8-element phased array core-chip with a reconfigurable number of output beams.
The reconfigurable chip contains 8-phased-array channels with a wideband input switching network and a reconfigurable output combining network. These input and output networks allow the chip to be configured for 4 different applications: 1) 8-antenna inputs with a single-beam output beamformer; 2) 4-antenna inputs with 2-simultaneous beamforming outputs; 3) 2-antenna inputs with 4-simultaneous beamforming outputs (example shown in Fig. 2). Additionally, the beamforming outputs can be mixed to an IF frequency before exiting the chip. Also, 4) additional mixers are placed on-chip so as to reconfigure the chip as a 2-antenna input digital beamforming receiver.

II. TWO-INPUT FOUR-BEAM OUTPUT CONFIGURATION

For this paper and due to the limited available space, we will present results on the 2-antenna input/4-beam output mode (Fig. 2), but all the other modes have similar response since they use the same core-channels. In this design, the signals are differential throughout the chip except at the RF input/output ports which are single-ended (SE). The conversion between the input SE ports and the differential circuitry is done using wideband active baluns (input) and Diff-to-SE converters (output). The input/output 2-16 GHz switches are designed to be either all passive using the 0.18μm CMOS technology available in this process, or using active cascode-based stages.

The 2-16 GHz channels consist of vector-modulator phase shifters (PS) based on a wideband quadrature all-pass filter network [1], and followed by a variable gain amplifier (VGA). Fig. 3 and 4 present the relevant circuits for the input active switch and vector modulator, respectively.

The channel outputs are then fed to an active 4-pole/4-throw switch to select the number of channels which are fed to the beamformer as shown in Fig. 1 and 2.

The left and right channels are first added together in a wideband active cascode summer, and these outputs pass by a switch network so as to be either added again for form 1 or 2 simultaneous beams, or routed to the output ports as 4 simultaneous beams (see Fig. 2). Note that the final summers in the 1 or 2 beam configuration are based on passive networks to maintain high linearity and avoid any power saturation in the output summer.
Fig. 5. 8-element phased array chip with reconfigurable number of beams (5 mm x 2.5 mm)

III. MEASUREMENTS

The chip was fabricated using the Jazz H4 SiGe BiCMOS process with 6-layer metal stack-up. The entire chip consumes 850 mA from a 2.5 V supply for all-modes, and the effective single channel power consumption is 265 mW. The chip size is 5x2.5 mm$^2$ (Fig. 5). The measured gain and input/output return losses (RL) are presented in Fig. 6. For the 2-antenna/4-beam configuration, the gain is defined as the measured $S_{21}$ between the output port and a single input port, with the other port left open.

The measured gain for the 2-in 4-out mode is ~10-11.5 dB at 2-16 GHz with excellent gain flatness (presented for the 0° phase setting). The chip results in a wideband input and output impedance match as shown in Fig. 6. The normalized channel phase responses are shown in Fig. 7 and no phase crossings are observed at 2-16 GHz for a 5-bit setting (an 8-bit control is also possible). The measured RMS gain and phase error (not shown) are < 0.4 dB and < 6° at 2-16 GHz, with a range of 3-4° at 6-12 GHz, ensuring a 5-bit phase response over the entire band (and a 6-bit response at 6-12 GHz). A 3-bit VGA with 8 dB linear-in-dB control with DAC circuitry is also present on each channel, and the results are not included for brevity. The chip noise figure and input referred $P_{1\text{dB}}$ ($IP_{1\text{dB}}$) are also measured over frequency (Fig. 8), and the NF is 11.5-12 dB at 2-14 GHz. The $IP_{1\text{dB}}$ is ~ -15±1 dBm and also shows a flat response. The NF and $IP_{1\text{dB}}$ values agree well with simulations to within ±1 dB. Note that other core-chip configurations result in similar gain, input and output match, NF and $P_{1\text{dB}}$ values since this is mostly limited by the input switching network and the output active combiners.

IV. CONCLUSION

This paper presented a wideband 2–16 GHz Phased Array Receiver chip with reconfigurable beam outputs. The chip performance is demonstrated over 2-in 4-out configuration to show its unique capabilities over a wide range of frequencies. Application areas are phased-array systems requiring a variety of beams, and using the same core-chip for reduced cost and system flexibility.

REFERENCES


