A Ring-HEMT for Improved GaN MMIC Thermal Dissipation

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Abstract — A novel GaN HEMT which reduces the junction temperature is presented. The new structure uses a ring-like layout for the gate stripes, aimed at increasing the separation between stripes. Simulation and experimental results indicate improved performance of the Ring-HEMT, stemming from thermal effects and their interaction with device parameters. Compared to a regular HEMT, the new HEMT showed a decrease in junction temperature of 40°C from 178 °C resulting in a significant improvement in output power, and 43\(^x\) fold increase in lifetime.

Index Terms — GaN HEMT, FET; Junction Temperature; Thermal Resistance; Reliability.

I. INTRODUCTION

Microwave HEMTs (High-Electronic Mobility Transistors) and MMICs have performance which is generally limited by the maximum allowable voltage/electric field, current density, and junction (or channel) temperature. Self heating within the device is undesirable as it reduces performance and lifetime [1]-[2]. The junction temperature \(T_j\) is correlated with the device lifetime through the Arrhenius equation [3], and may be determined through simulations [4]-[6], theoretical models [7]-[8], or experiments [9]-[11]. Junction temperature directly affects the bandgap of the electronic material, carrier mobility, carrier saturated velocity, which in turn influence the device’s pinch-off voltage, breakdown voltage, transconductance, saturation current, output power, and noise performance [12]. Reducing \(T_j\) typically leads to enhanced device performance, and reliable, sustainable operation. Self heating in transistors also leads to memory effects [13] which cause linearity performance degradation. Junction temperature is directly proportional to power dissipation through the thermal resistance value (which has some temperature dependence due to the nonlinearity of the thermal conductivity). It also depends critically on the device layout. In the case of field effect transistors (FETs) and high electron mobility transistors (HEMTs), \(T_j\) increases with the thermal resistance constant, and depends on the gate-width, gate-length, gate-pitch, and substrate thickness and thermal conductivity [8]. GaN-based power devices have demonstrated a high performance capability, yet their full microwave performance is still limited by thermal effect and its interaction with device parameters. A study on a new device layout was initiated to offer a different approach to address these thermal related issues. In this paper, a novel technique for reducing junction temperature is presented with experimental and simulation results. The technique focuses on re-arranging the gate-stripes into a ring-like layout, and increasing the separation among them, thereby reducing heat crowding. Simulations and experimental verification indicate a significant heat reduction as a result of the new design, leading to improvement in device microwave performance.

II. PRINCIPLE OF OPERATION OF THE NEW HEMT

Consider a HEMT with constant highly localized heat sources (Fig. 1) on a substrate (say SiC) of thickness \(t\). The heat sources represent the gates of the device with length, \(L_g\), and width, \(W_g\). The gate pitch is \(s\), while thermal conductivity the material is \(k\).

The junction temperature may be calculated using numerical analysis [6], or the closed form expression in [8]. The temperature in each stripe is determined by (a) the self heating of the gate stripe, and (b) the cross heating from

Fig. 1. HEMT parameters description. Gate dimensions are \(L_g \times W_g\), gate pitch \(s\), substrate thickness is \(t\).

Fig. 2. (a) Regular HEMT layout, showing two signal paths, (b) Ring-HEMT layout. Gate stripes are highlighted with a black line to show their locations.
nearby gate stripes. Reducing the self heating can be achieved by increasing the gate length \(L_g\), and decreasing substrate thickness, \(t\), and power dissipation per millimeter gate-width, \(P_{mm}\). However, in a typical fabrication process, \(L_g\) and \(t\) cannot be readily changed. Reducing \(P_{mm}\) by increasing power-added-efficiency is a well recognized goal [13]. Minimizing cross heating from neighboring stripes can be achieved by increasing the gate pitch, \(s\). This comes at the expense of a larger device area, leading to (1) wider drain islands (hence, larger drain-source capacitance \(C_{ds}\)), (2) wider source islands (hence, greater source inductance \(L_s\)), and (3) increased phase difference of signal paths among the gate stripes (e.g., between path \(P_1\), and \(P_2\) in Fig. 2). Increasing \(C_{ds}\), and \(L_s\) usually reduces bandwidth, gain (due to negative feedback from \(L_s\)), and makes output matching more difficult. The phase difference also reduces output power and gain. These effects become more significant at mm-wave frequencies.

This paper proposes reducing junction temperature by re-arranging the gates into a ring-like layout, Fig. 2. A regular HEMT with 0.25 \(\mu\)m gate length, 600 \(\mu\)m (8 \(\times\) 75 \(\mu\)m) gate periphery, 28.5 \(\mu\)m gate pitch, dissipating 6 W (30 V \(\times\) 200 mA) is shown in Fig. 2(a). A Ring-HEMT with the same gate periphery, 600 \(\mu\)m, is shown in Fig. 2(b). As the Fig. 2(b) shows, the distance is maximized between the gates while keeping the paths length for all stripes roughly equal. The increase in the core area, compared to a regular HEMT, is about 50%. With the increased area, some of the internal capacitances are expected to increase. However, that may be tolerated in favor of a lower junction temperature, especially for wide bandgap semiconductors (such as GaN, and SiC) where the performance (gain, output power, and noise) is frequently limited by heat dissipation, not the intrinsic device capability. The temperature, \(T\), and voltage, \(V\), variation inside the device are similar in that both follow Laplace’s equation. To reduce \(T\) (analogous to \(V\)), the heating elements (analogous to electric charges) should be distributed similar to electric charges on a conducting disk. For a conducting disk at a fixed voltage, the distribution of charge concentrates around the edges, as shown in Fig. 3(a). Ideally, the heating elements should be positioned in a similar way (less heating in the center, more at the edges) in order to achieve constant \(T\) (similar to constant \(V\)). This is what inspired the current layout.

A numerical simulator (ANSYS), with nonlinear thermal conductivity, was used to calculate the junction temperature for the regular HEMT, and the Ring-HEMT, Fig. 3(b), assuming a base plate temperature of 25 °C. The temperature in the regular HEMT reaches 178.2 °C, while the Ring-HEMT reaches 138.1 °C, under the same power dissipation. That is equivalent to a 30% drop in thermal resistance which is very significant in terms of reliability [1]. Consider the Arrhenius equation:

\[
\ln \left( \frac{MTF_2}{MTF_1} \right) = \frac{E_a}{k_b} \left( \frac{1}{T_2} - \frac{1}{T_1} \right),
\]

where MTF\(_{1,2}\) is the mean-time-to-failure or (MTTF), \(E_a\) is the activation energy, \(T_{1,2}\) are the absolute temperature in degree Kelvin, and \(k_b\) is the Boltzmann constant \((8.6 \times 10^{-5} \text{ eV/K})\).

Fig. 3. (a) Charge distribution on a conducting disk at fixed voltage. (b) Channel temperature along center line for both regular HEMT (solid line), and Ring HEMT (dashed line).

Fig. 4. Pictures of a regular HEMT and a Ring-HEMT.

Fig. 5. (a) Change in cutoff frequency as the drain voltage is increased (the drain current was kept constant at 200 mA, 40% of \(I_{ds}\)). (b) Change in output power \((P_{\text{out}})\) as the drain voltage is increased.

Fig. 6. Sample power drive curves for a regular HEMT, and a Ring HEMT, \(V_d = 25\) V.

| TABLE I |
| EXTRACTED EQUIVALENT CIRCUIT CAPACITANCES (PF/MM) |
| Type   | \(C_g\) | \(C_d\) | \(C_p\) |
| Reg. HEMT | 0.710  | 0.14   | 0.09   |
| Ring HEMT | 0.711  | 0.23   | 0.14   |

Evaluating the expression for GaN with \(E_a = 1.5\) eV [14], \(T_1 = 138.1\) °C, \(T_2 = 178.2\) °C, gives \(MTF_2 / MTF_1 = e^{1.77} = 43.4\). That is, the improvement in lifetime is 43\(\times\) fold.

For a power amplifier (PA) MMIC, with the new device layout, the overall area of the MMIC would only increases slightly. Consider, for example, the layout of the
representative MMIC with dimensions 2.8 × 2.1 mm (area = 5.9 mm²). The active devices occupy about 0.22 mm², less than 4% of the total area. Hence, even if the area of each HEMT was increased by 100%, the total increase in MMIC area would be around 4% only. An alternative approach to reducing the temperature is to increase the gate pitch. However, to achieve similar temperatures to those of the Ring HEMT, the gate pitch will need to be quadrupled and, consequently, the area will quadruple. Additionally, the paths length difference (e.g., between P₁ and P₂, Fig. 2A) will be severe, and the increase in Cds and Ls will be multi-fold.

III. EXPERIMENTAL RESULTS

AlGaN/GaN HEMTs were fabricated to validate the new concept. The AlGaN/GaN epitaxial layers were fabricated on MOCVD grown 3-inch semi-insulating 6H-SiC substrates. The material has an AlN nucleation layer on SiC substrates. The epitaxial layers consist of an undoped GaN channel layer, an AlN barrier layer, an undoped AlGaN layer, and a GaN cap layer. Device isolation were formed by mesa etch using reactive-ion-etching (RIE). Ti/Al-based metal stack and RTA (Rapid Thermal Anneal) were used for source and drain ohmic contacts. Gate openings were defined by e-beam lithography.

Pictures of a regular HEMT and a Ring-HEMT are shown in Fig. 4. Fig. 5(a) shows the cutoff frequency f₁ as a function of bias for the Ring-HEMT along with that of the regular HEMT. An approximate expression for the cutoff frequency is

\[ f₁ = \frac{gₘ}{2\pi (C_{gs} + C_{gd})} \]

where gₘ is the transconductance, Cgs is the gate-source capacitance, and Cgd is the gate-drain capacitance. As the figure indicates, f₁ drops with drain voltage (the bias current is kept constant at 200 mA) due to heating, as expected. However, the rate of deterioration of f₁ with bias is greater for the regular HEMT. Additionally, at full bias (30 V), the difference of f₁ between the regular HEMT and the Ring-HEMT is insignificant. In fact, the Ring-HEMT slightly outperforms the regular HEMT. The equivalent circuit was extracted to find the internal capacitances. Table I shows the extracted capacitance values (per mm) of gate-source capacitance Cgs, gate-drain capacitance Cgd, and drain-source capacitance Cds. The increase in capacitances is moderate. The growth of capacitances may be reduced through a revised layout. The Ring-HEMT and the regular HEMT were tested in a load-pull setup at 10 GHz. The load was optimized at 20 V drain voltage, and 40% Ls for both devices; both have the same gate periphery and thus, the same drain current density. Then, the gate voltage and load were kept fixed to mimic HEMT use in a typical MMIC circuit. Fig. 5(b) shows the measured P₁dB and Fig. 6 shows a sample power drive curve. At low bias (10 V), the output power for both HEMTs are similar. However, the regular HEMT’s output power deteriorates quickly with drain voltage. The observed change in P₁dB is caused by heating, and the input/output matching variation with drain voltage and drive level, especially since the input/output capacitances of GaN HEMTs are known to be bias dependent. It should be noted that thermal and electrical effects are inter-related and determining the contribution of each is an open question for researchers. Both effects influence and provide feedback to each other. As the drain voltage was increased, the power gain of the regular HEMT started to compress more than the Ring-HEMT.

The Ring-HEMT consistently outperforms the regular HEMT at higher biases. Three devices were measured of each type and similar improvements in performance were obtained.

REFERENCES

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