Fully Integrated Switchable Filter Banks

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Abstract — Fully integrated switchable filter banks at S-band have been successfully demonstrated using a radiation hardened CMOS SOI process in conjunction with an aluminum nitride (AlN) microresonator process. Single pole-multi throw switches were developed in the CMOS SOI process through a series of multi-project wafer runs while the filters were developed using aluminum nitride based microresonators. Each had separate yet concurrent design cycles and was demonstrated separately prior to integration. After design improvements to both technologies, a full monolithic integration was implemented of the microresonator filters with the CMOS switches, showing the compatibility of the two technologies. A four channel single chip switchable bank of ~7MHz bandwidth filters at S-band was demonstrated exhibiting approximately 8 dB of insertion loss and 60dB of stop band rejection.

Index Terms — CMOS, MEMS, filters, switches

I. INTRODUCTION

Advanced communications systems are driving the need for fully integrated solutions. From RFIC technology to multi-chip modules, integration and miniaturization is the focus. One technology highly desired by communication systems designers is a wide range of narrowband filters with specific stopband characteristics as well as the ability to switch easily among this bank of filters. Switchable filter banks represent a critical technology gap for realizing the next generation of communication systems. Microfabricated resonators offer a smaller, more highly integrated filter technology than what is available using traditional bulk or surface acoustic wave (BAW or SAW) techniques which are hindered by fabrication limitations. Microresonator filters can realize arrays of filters from 20 MHz to several GHz on a single chip [1] and can be monolithically integrated with CMOS technology without altering the CMOS fabrication process. This integration ability is fundamental to providing a switchable array of narrowband filters leading to higher reliability and lower component count. As a result of innovative research and development, a single chip solution providing a switchable filter bank has been demonstrated.

II. CMOS SWITCHES

Switches were designed in Sandia’s radiation hardened CMOS SOI process using partially depleted MOSFETs, where previously no S-band switch had been demonstrated. For this application, a body-source tie was implemented. Partially depleted MOSFETs are similar in behavior to bulk devices which simplify modeling to a certain extent [2]. This process features a five level metal stack-up and uses chemical mechanical polishing (CMP) for planarization.

Prior to this project, no RF CMOS model existed for this process and only modest work had been done with RF integrated circuits (RFICs). The model used for these designs was the BSIMSOI3 which offers an option for a partially depleted mode and was developed from the BSIM3 by adding SOI effects [2]. Using Agilent’s IC-CAP modeling software and an existing DC BSIMSOI3 model, RF sized devices (widths >50μm) were measured and the BSIMSOI3 RF parameters were extracted.

A. Switch Designs and Results

The switch design had requirements for an insertion loss of < 5dB and a desired isolation of 25dB. A series-shunt configuration using one series and one shunt transistor for each path resulted in the right tradeoff between insertion loss and isolation at S-band (2-4GHz). Two designs had a series transistor width of 300μm (12x25μm fingers) with a shunt transistor width of 150μm (6x25μm) for one design and 300μm (12x25μm) for the other design; both had gate lengths of 0.35μm. An input inductor was added for matching to 50-ohms and output coupling capacitors were on each switch leg. These configurations were used to design and fabricate SPDT, SP3T and SP4T switches using NMOS transistors.

The first iteration resulted in varying degrees of functionality where the functioning path(s) had very poor insertion loss (10dB) compared to simulated (1dB). The deviation from the simulated response in both magnitude and phase was attributed to the CMP process, which uses a metal fill and then polishes to obtain a planar surface for the next process step. This extra metal surrounding all the structures increases parasitics by adding capacitance and series resistance to the circuit behavior. On the first fabrication run, only the inductor had a protect layer surrounding it blocking it from the CMP metal fill, as seen in Fig. 1a.

![Fig. 1. SPDT CMOS switches with and without CMP fill](image)

For subsequent runs, the CMP metal fill was excluded from the entire circuit area (Fig. 1b) and minor tweaks were made...
to the layout, resulting in insertion losses ranging from 1.6dB to 3.1dB and 22dB to 24dB of isolation. The superior performance was layout dependent, favoring designs that were more symmetric and had fewer elements, decreasing complexity and thus crosstalk and coupling between metal lines.

III. MICRORESONATOR FILTERS

Because of their high-Q and temperature stability [3], microresonators enable on-chip, narrowband RF channel selection that no existing filter technology can perform. High-Q microresonators can form complex filtering functions, realize multiple frequency filters in a small size on a single substrate, and can be monolithically integrated with the CMOS switches needed to perform RF channel selection, offering interconnect and size reductions. Scaling of the microresonators to S-band frequencies from UHF band required numerous technical advances, specifically in the areas of fabrication and acoustic/electrical modeling.

A. Frequency Scaling and Device Thickness

A microresonator filter is formed here by electrically coupling two microresonators together; each resonator occupies 120 x 246 μm² of die area (Fig. 2a). A typical cross section of a microresonator is shown in Figure 2b. The microresonator is constructed of a piezoelectric aluminum nitride (AlN) material sandwiched between two metal (Al) electrodes. A bottom dielectric layer (SiO₂) is also shown that provides temperature compensation.

A previous process used to fabricate lower frequency resonators [4] was altered for this work; Table I displays the device design changes necessary to enable high performance S-band filter arrays. The filter arrays were optimized for a total film thickness of < 0.35 for the highest frequency filter in the array, avoiding any thickness dependencies that lead to the degradation of bandwidth or insertion loss. The reduction of spurs is also correlated to the thickness of the resonators and is carefully chosen to help eliminate spurs [5]. Advanced acoustic models were developed to study the spurious modes and performance as the resonator thickness to wavelength ratio becomes finite. Other techniques employed for spur mitigation include coupling resonator stages in series and using stubbed electrodes.

The inset of Figure 3 shows the first generation filters that had 8.6dB insertion loss and ~9MHz bandwidths. Figure 3 shows a second generation filter bank on CMOS with 6dB insertion loss and narrower bandwidths of < 7 MHz (Fig. 3), demonstrating improvement over the first iteration of filters. Processing improvements resulting in a vertical AlN sidewall were developed and demonstrated to reduce insertion loss and improve quality factor. Vertical sidewall etching was a major technical advance that showed promising improvements. Resonator design improvements, such as using multiple stages, were made to reduce spurs and to improve filter isolation. These filters demonstrated few spurs and had stop band rejections in excess of 50 dB over a 2.5 GHz bandwidth.

![Photo of microresonator filter](image1)

**Fig. 2.** Photo of microresonator filter and cross-section of microresonator

![Cross-section of microresonator](image2)

**Fig. 3.** Measured response of an S-band filter array with 6.2-8.0dB insertion loss, ~7MHz bandwidths and stopband rejections of >50dB with no flyback; Measured response of initial S-band filter, inset.

<table>
<thead>
<tr>
<th>Material</th>
<th>Low Frequency Device Thickness</th>
<th>S-Band Device Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>825 nm</td>
<td>110 nm</td>
</tr>
<tr>
<td>Bottom Metal (Ti/TiN/Al)</td>
<td>20/50/100 nm</td>
<td>20/50/50 nm</td>
</tr>
<tr>
<td>AlN</td>
<td>750 nm</td>
<td>400 nm</td>
</tr>
<tr>
<td>Top Metal (Al/TiN)</td>
<td>200/50 nm</td>
<td>100/50 nm</td>
</tr>
<tr>
<td>Total Thickness</td>
<td>1995 nm</td>
<td>780 nm</td>
</tr>
<tr>
<td>Min. Wavelength</td>
<td>5700 nm</td>
<td>2230 nm</td>
</tr>
<tr>
<td>Approx. Max. Freq.</td>
<td>1.75 GHz</td>
<td>4.5 GHz</td>
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</tbody>
</table>
IV. MONOLITHIC INTEGRATION

Realizing these switchable filter banks requires exploiting the unique properties of microresonators to form complex filter architectures and monolithic integration of S-band filter banks with low loss radiation hardened channel select switches. Commercially available monolithically integrated switchable filter banks at S-band do not exist. The microresonator filters were fabricated atop the CMOS wafers after the completion of the top metal layer; a single chip switched filter array can be seen in Figure 4. Although the filters can be fabricated directly over the switches, the layout below (Fig. 4) showed superior performance.

Among the multi-throw switch designs, the SP4T switched filter array had the best performance showing insertion loss of 7 to 8.8dB, <7MHz bandwidth (Fig. 5) and varying degrees of isolation. The SP4T design had 20 to 25dB measured isolation for all but port 2, which was about 11dB; this can be attributed to layout issues. The switch filter array had excellent return loss of 22 to 35dB (inset, Fig. 5). The filters used in the integration were nominal as the process equipment that produced the superior vertical sidewall was unavailable, resulting in slightly higher overall insertion loss.

The group delay variation can be seen in Fig. 6 which shows an approximate value of 45ns at band center for this filter.

![Fig. 4. Photo of the single chip SP4T switched filter array showing switch (left) and filters (right).](image)

![Fig. 5. Measured insertion loss of 7 to 8.8dB of same filter array; measured return loss of 22 to 35dB of an S-band switched microresonator filter array, inset.](image)

![Fig. 6. Group delay of one switched filter](image)

Fig. 4. Photo of the single chip SP4T switched filter array showing switch (left) and filters (right).

Fig. 5. Measured insertion loss of 7 to 8.8dB of same filter array; measured return loss of 22 to 35dB of an S-band switched microresonator filter array, inset.

The group delay is similar across all switched filters ranging from 42ns to 48ns. As with many communications systems, the part to part group delay variation is more critical than the value itself and these switched filters show promise in this area.

V. CONCLUSION

A fully integrated switchable filter bank has been successfully demonstrated, offering a monolithic solution for what is currently a multi-chip application.

REFERENCES