A Miniature Q-band CMOS LNA with Quadruple-Cascode Topology

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Abstract — In this paper, a miniature Q-band low noise amplifier (LNA) is fabricated for demonstration using 90-nm Low Power (LP) CMOS technology. The quadruple-cascode topology is applied to achieve a high gain performance with a compact chip size. Besides, a transformer is placed between the cascode devices to reduce the noise figure and enhance the stability and also bandwidth of the LNA. The LNA features a maximum small signal gain of 20.3 dB and a minimum noise figure of 4.6 dB at 40 GHz, with a power consumption of 15 mW. The chip size is only 0.48 × 0.44 mm², including all the testing pads. To the best of our knowledge, this is the first quadruple-cascode LNA in millimeter-wave (MMW) regime reported to date.

Index Terms — Low noise amplifier, cascode, CMOS, MMIC.

I. INTRODUCTION

With the growing demands of wideband local area network (WLAN) and high data rate communications systems lead to the development of wideband receiver and transmitters becomes very popular. In a RF front-end receiver, low noise amplifier dominates the signal-to-noise ratio of the system. The design of CMOS LNA should make best trade-off between noise figure, gain, power consumption and chip area. The common-source (CS) configuration with source degeneration inductor [1] and transformer feedback [2] is usually used to implement CMOS LNAs to achieved low noise figure and high gain performance at low frequency. However, a single-stage CS LNA suffers from gain insufficient at microwave frequency. Hence, multiple cascade stages can be used to achieve high gain performance as reported in [3]-[4]. This topology will result in not only higher noise figure, larger chip area, and also higher power consumption. In [12] CPW transmission line is used to reduce the loss from passive components comparing with thin film micro-strip transmission line (TFML), however, this approach also suffers from gain insufficient problem. The cascode topology becomes popular in designing CMOS LNA at microwave frequency in recent years [5]-[9]. In [8], cascode configuration shows better frequency response and more compact size at microwave frequency due to the absence of Miller effect. However, the common-gate stage will contribute considerable noise as the operation frequency increase to microwave frequency in cascode or multi-cascode topology. The quadruple-cascode topology was proposed to implement a high gain linear power amplifier at 2 GHz in [10]. To reduce the noise contribution of CG stage in cascode configuration, a parallel inductor [11] or a series inductor [13] was used to resonate with the parasitic capacitance of cascode topology, but occupied large area and also suffered from low gain. In this paper, another approach is proposed to reduce the noise and enhance the bandwidth of the quadruple-cascode configuration at microwave frequencies. A transformer is designed to place between the cascode devices to minimize the noise figure and enhance the stability and also bandwidth of the LNA. Based on the quadruple-cascode structure with noise reduced technique, a single-stage CMOS LNA achieves a small signal gain of 20 dB and NF of 4.6 dB at 40 GHz, with a miniature chip size of 0.48 × 0.44 mm². The total power consumption is 15 mW. This is the first quadruple-cascode LNA in MMW regime reported to date.

II. CIRCUIT DESIGN

The LNA is fabricated in TSMC commercial 90-nm low power (LP) CMOS technology, which provides one-poly-nine-metal (1P9M), with ultra thick metal of 3.3-µm. Metal-insulator-metal (MIM) capacitors and polysilicon resistors are available. The $f_{\text{max}}$ and $f_t$ of the CMOS process are 110 GHz and 130 GHz, respectively. In general, the cascode structure features a higher maximum stable power gain (MSG) than the common-source configuration. Also, the quadruple-cascode configuration presents a higher MSG than the cascode and triple-cascode cells. The schematics of the cascode, the triple-cascode and the quadruple-cascode devices are shown in Fig.1.

Fig. 1. (a) Cascode device, (b) triple-cascode device, and (c) quadruple-cascode device.
The quadruple-cascode cell consists of a common-source transistor, $M_1$, and three common-gate transistors, $M_2$, $M_3$, and $M_4$. The combinations of the device size are chosen similar to the method reported in [9]. The transistor $M_1$ is selected to be 16 finger NMOS with total gate width of 40 µm. $M_2$, $M_3$, and $M_4$ are 24 finger NMOS with total gate width of 60 µm, 32 finger NMOS with total gate width of 80 µm, and 40 finger NMOS with total gate width of 100 µm, respectively.

Under class-A bias condition, the simulated MSG/MAG and minimum noise figure (NF$_{min}$) of the cascode devices are shown in Fig. 2. It is observed that the quadruple-cascode device presents a MSG of 30.5 dB and a NF$_{min}$ of 4.4 dB at 40 GHz. The triple-cascode device has a MSG of 20 dB and a NF$_{min}$ of 3.6 dB, while the cascode device has a MSG of 16.3 dB and a NF$_{min}$ of 3.0 dB. Although the quadruple-cascode device shows better MSG than the cascode and triple-cascode devices, it suffers higher NF$_{min}$ than the cascode and triple-cascode devices.

![Fig. 2. Simulated MSG/MAG and NF$_{min}$ of the cascode, triple-cascode and quadruple-cascode devices.](image)

Figure 3 shows the circuit schematic of the proposed Q-band LNA with single-stage quadruple-cascode topology. In order to reduce the noise contributed by $M_2$, $M_3$, and $M_4$, a transformer consisting of three inter-stage inductors $L_1$, $L_2$, and $L_3$ are designed to place between the quadruple-cascode devices. As shown in Fig. 1, $L_1$ is placed between two NMOS transistors $M_1$ and $M_2$; $L_2$ is placed between two NMOS transistors $M_2$ and $M_3$; and $L_3$ is placed between two NMOS transistors $M_3$ and $M_4$. At MMW bands, the parasitic capacitances ($C_{gs}$-$C_{gd}$) of $M_2$, $M_3$, and $M_4$ will cause extra noise at the output port in Fig. 1. By adding the transformer to the cascode cell, $L_1$, $L_2$, and $L_3$ incorporate with the parasitic capacitances as resonators, and hence the parasitic capacitances of the common-gate stages can be resonated out. $L_1$ is selected to be 0.08nH, while $L_2$ and $L_3$ are 0.12, and 0.16nH, respectively. The coupling factors of $L_1$ and $L_2$, respectively.

The quadruple-cascode cell is selected as 0.59 ($k_{12}$ = 0.59). The coupling factors of $L_1$ and $L_2$ is selected as 0.43 ($k_{13}$ = 0.43), and the coupling factors of $L_2$ and $L_3$ is selected as 0.21 ($k_{34}$ = 0.21). Using the parameters we selected above, the quadruple-cascode cell is stable above 40 GHz. However, the MSG of quadruple-cascode cell suffers some decrement below 40 GHz. In the mean while, the NF$_{min}$ is reduced from 4.4 to 3.1 dB. With transformer consisting of $L_1$, $L_2$, and $L_3$, the noise figure is minimized and the quadruple-cascode configuration can be applied to implement the Q-band LNA.

![Fig. 3. Circuit schematic of the proposed Q-band LNA.](image)

Each gate is biased through a 10-kΩ resistor. A shunt inductor $L_4$ and a series inductor $L_3$ are utilized to simplify and implement the input matching network. In addition, a shunt inductor $L_5$ and a series inductor $L_6$ are utilized to simplify and implement output matching network. The input network is matched for the minimum noise figure, and the output is conjugately matched for the maximum small signal gain. All the matching networks are formed with inductors, so that they can be easily realized to achieve a compact layout. Since the quadruple-cascode configuration is more unstable due to its high power gain, the inter-stage inductors $L_1$, $L_2$, and $L_3$ should be designed carefully for unconditional stability. The chip photograph is presented in Fig. 4 with a die size of $0.48 \times 0.44$ mm$^2$, including all the testing pads.

### III. MEASUREMENT

The quadruple-cascode LNA was measured via on-wafer probing using Agilent HP8510 test set. Figure 5 shows the measured small signal gain and return losses of the proposed LNA. It is observed that the LNA has a measured peak gain of 20 dB at 40 GHz, with the input return loss of 20 dB and the output return loss of 20 dB. The 3-dB bandwidth is from 32 to 44 GHz. Within the 3-dB bandwidth, the input and output
return losses are better than 10 and 5 dB, respectively. The measured reverse isolations are all better than 30 dB from 32 to 44 GHz. Figure 6 illustrates the measured noise figure. The LNA has a noise figure of 4.6 to 5.2 dB from 34 to 44 GHz. At 38 GHz, the measured input 1-dB compression point (IP_{1dB}) is -18 dBm as shown in Fig. 7. The LNA has an output P_{1dB} of 1.5 dBm with a total power consumption of 15 mW. Table I summarizes the previously reported CMOS Q-band LNAs and this work. The single-stage quadruple-cascode LNA achieves a miniature size and high gain performance with low noise figure and low power consumption. The figure of merit (FOM) is used to compare between the proposed design and recently published wideband CMOS LNAs, which was originally proposed in [14], [15] for wideband LNAs, and is modified here to consider the output power of LNAs by replacing the IIP3 term by the OP_{1dB}.

\[
FOM = \frac{\text{Gain (dB)} \times \text{Bandwidth (GHz)} \times \text{OP}_{1dB} (\text{mW})}{[\text{NF (dB)} - 1] \times \text{P}_{dc} (\text{mW})}
\]

Fig. 4. Chip photograph of the LNA with the area of 0.211 mm².

Table I

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<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>Bandwidth (GHz)</th>
<th>NF (dB)</th>
<th>OP_{1dB} (mW)</th>
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</table>

Our amplifier is the first quadruple-cascode LNA in MMW regime reported to date and features the highest FOM.

Fig. 5. Measured small signal gain and return losses of the proposed LNA.

Fig. 6. Measured NF of the proposed LNA.

Fig. 7. Measured gain and P_{out} v.s P_{in} of the proposed LNA.

*TF stands for transformer
IV. CONCLUSION

A miniature Q-band LNA with quadruple-cascode topology was designed and fabricated in TSMC commercial 90-nm Low Power (LP) 1P9M CMOS process. Based on the quadruple-cascode configuration with noise reduced transformer, the proposed LNA has a measured peak gain of 20 dB and a NF of 4.6 dB at 40 GHz. This LNA achieves an excellent performance with 3-dB bandwidth from 32 to 44 GHz among all the CMOS Q-band LNAs reported to date. Moreover, the CMOS LNA presents a low power dissipation of 15 mW, with a chip size of 0.211 mm².

ACKNOWLEDGEMENT

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REFERENCES


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