Electro-thermal Simulation of 1200 V 4H-SiC MOSFET Short-Circuit SOA†

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Abstract—The purpose of this paper is to introduce a dynamic electro-thermal simulation and analysis approach for device design and short-circuit safe-operating-area (SOA) characterization using a physics-based electro-thermal Saber®* model. Model parameter extraction, simulation, and validation results are given for several commercially available 4H-silicon carbide (SiC) power MOSFETs with a voltage rating of 1200 V and with current ratings of 31.6 A and 42 A. The electro-thermal model and simulations are used to analyze the short-circuit SOA including the measured failure time (t_{failure}) and simulated device internal junction temperature (T_j) at failure for different gate voltages (V_{GS}) and drain voltages (V_{DS}).

Keywords—electro-thermal simulation; model validation; MOSFET; short-circuit; silicon carbide; SOA

I. INTRODUCTION

Short-circuit withstand time is an important attribute of power semiconductor devices that enables rugged performance of power electronics systems for many applications [1, 2]. Although the higher intrinsic temperature of wide-bandgap (WBG) semiconductors provides some advantage in short-circuit performance, this is outweighed by the much more rapid heating of the voltage blocking layer due to the thinner voltage blocking layers and smaller die area which are otherwise a key advantage of WBG power devices. The purpose of this paper is to introduce a dynamic electro-thermal simulation and analysis approach for device design and short-circuit SOA characterization using a physics-based electro-thermal Saber® model. Model parameter extraction, simulation, and validation results are given for several commercially available, 1200 V, 42 A (0.12 cm²) referred to as Type-A in this work and 1200 V, 31.6 A (0.06875 cm²) referred to as Type-B, 4H-SiC power MOSFETs at different V_{GS} and V_{DS}. The electro-thermal model and simulations are used to analyze short-circuit SOA including t_{failure} and T_j.

II. APPROACH

A. Circuit Configuration of the Short-Circuit Test

Fig. 1 shows the short-circuit measurement setup used for the MOSFETs. The DC bus voltage across the capacitor bank (C_{bank}) is set prior to the short-circuit event. The short-circuit current is measured as the voltage across the sensing resistor (R_{sense} = 0.05 Ω). The circuit uses an isolated gate drive (represented by the transformer) [3] to drive the device under test (DUT). The V_{GS} pulse amplitude is controlled by using the adjustable power supply and a zener clamp diode to provide a rectangular pulse that is referenced to the source of the DUT. For simplicity, the parasitic inductances (i.e., load inductance, stray inductance, and gate inductance) are not included in Fig.1 but they are characterized and included in the simulation circuit.

Fig. 1: Short-circuit measurement setup for 1200 V 4H-SiC MOSFETs.

B. Short-circuit Characteristics

Fig. 2 left graph shows the MOSFET drain-source voltage (V_{DS}), drain current (I_{D}), junction temperature (T_j), and total dissipated heating power (Q_{Total}). The right graph shows the Hefner chip thermal network component model [4, 5] that is modified to include 4H-SiC temperature dependent thermal properties of 4H-SiC and to include a higher density of thermal nodes. The higher density of thermal nodes is needed due to the higher material field strength of 4H-SiC, which results in thinner voltage blocking layers and thus higher power dissipation densities. This chip thermal network component model distributes the dissipated heat (Q = E·J) in the trapezoid determined by the dopant density and thickness of the voltage blocking layer.

For the pre-existing short-circuit tests discussed in this paper, the gate voltage is switched on while the drain remains shorted to the high-voltage supply with low impedance as shown in Fig. 1. This results in a high drain current with the drain voltage remaining relatively constant at the high-voltage rating.

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Type-A is used to designate 1200 V, 42 A SiC MOSFET: http://www.cree.com/~/media/Files/Cree/Power/Data%20Sheets/CMF20120D.pdf.

Type-B is used to designate 1200 V, 31.6 A SiC MOSFET: http://www.cree.com/~/media/Files/Cree/Power/Data%20Sheets/C2M0080120D.pdf.

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supply value. Consequently, the voltage blocking region (drift region) of the MOSFET undergoes rapid adiabatic heating (i.e., heat does not diffuse significantly to surrounding regions during the event) as shown in Fig. 2.

To accurately model the electrical characteristics of short-circuit events, an extended model parameter extraction procedure is used to extract the temperature dependence of the saturation region transconductance parameter \( K_{psat} \) and channel length modulation parameter \( (\lambda) \) of the Hefner dynamic electro-thermal insulated gate bipolar transistors (IGBT) /MOSFET model \([6, 7]\) for the high-current, high-voltage, and high-temperature conditions that occur during short-circuit events. Equation (1) is used for the MOSFET saturation current.

\[
I_{MOS,sat} = \frac{K_{psat}}{2} (V_GS - V_T)^2 [1 + \lambda (V_DS - V_GS + V_T)]
\]

(1)

The values of \( K_{psat} \), threshold voltage \( (V_T) \) and their temperature coefficients in the Hefner IGBT/MOSFET models are typically extracted using the IGBT Model Parameter extrACtion Tools (IMPACT) \([8]\) with a pulsed curve tracer and a temperature controlled test fixture. However, the temperature and drain voltage during short-circuit events go well beyond the practical ranges of this approach. Therefore, the IMPACT tools are supplemented with measurements using the low inductance test fixture as shown in Fig. 1 to extract the high temperature and high voltage dependence of the model parameters.

III. SHORT-CIRCUIT VALIDATION RESULTS

Figs. 3 and 4 are examples of the high temperature \( K_{psat} \) parameter extraction for the temperature coefficients of (2). It should be noted that the temperature dependence can be bimodal (increasing and then decreasing) as in Fig. 3 or can be monotonically decreasing depending on the device type:

\[
K_{psat} = \frac{K_{psa} \cdot 300}{1 + K_{ps2} \cdot \left( \frac{V_T}{T} \right)^2 + K_{ps3} \cdot \left( \frac{300}{T^2} \right) \cdot V_T}
\]

(2)

where, \( K_{psa}, K_{ps2}, \) and \( K_{ps3} \) are transconductance parameter factors at room temperature, and \( K_{ps1}, K_{ps4}, \) and \( K_{ps5} \) are temperature coefficients of the transconductance parameter factors.

In Figs. 5 and 6, the short-circuit SOA is defined in terms of the application voltages \( (V_GS \) and \( V_DS) \) for the failure events of Figs. 7-12 by plotting the short-circuit \( t_{failure} \) versus \( V_DS(V_GS - V_T)^2 [1 + \lambda (V_DS - V_GS + V_T)] \). The solid reference curve (purple line) is for \( t_{failure} = M_{sc}/V_DS(V_GS - V_T)^2 [1 + \lambda (V_DS - V_GS + V_T)] \). This enables a straight-forward calculation of the short-circuit withstand time based on application voltages \( (V_GS \) and \( V_DS) \) and basic model parameters \( (V_T \) and \( \lambda) \), where the more complex adiabatic heat source distribution, failure temperature, and temperature dependence of \( K_{psat} \) are lumped into the single short-circuit figure of merit value \( M_{sc} \). Minimizing the value of \( \lambda \) also improves short-circuit SOA.

Figs. 7-12 compare measured and simulated short-circuit failure waveforms for three different gate voltages and three different drain voltages for both Type-A and Type-B devices. Figs. 13 and 14 show the simulated internal temperature where each device failed for the short-circuit events. It should be noted that the failure temperature is chosen to be the hottest location in the chip (top thermal node in the model) at the \( t_{failure} \), which is identified by the time when the current starts to go vertical just before destruction in Figs. 7, 9, and 11 for Type-A devices and Figs. 8, 10, and 12 for Type-B devices. Therefore, the devices may be beyond the safe turn-off condition at a time prior to the identified \( t_{failure} \) event. On average, the failure temperature is approximately 650 °C ± 100 °C, and increases slightly with gate voltage for both Type-A and Type-B devices.
Fig. 5: Failure time versus normalized power dissipation density $V_{DS}(V_{GS} - V_T)^2[1 + \lambda (V_{DS} - V_{GS} + V_T)]$ graph for ten different 1200 V, 42 A 4H-SiC MOSFETs. The short-circuit figure of merit value is $M_{SC} = 2.65$ for Type-A.

Fig. 6: Failure time versus normalized power dissipation density $V_{DS}(V_{GS} - V_T)^2[1 + \lambda (V_{DS} - V_{GS} + V_T)]$ graph for nine different 1200 V, 31.6 A 4H-SiC MOSFETs. The short-circuit figure of merit value is $M_{SC} = 1.85$ for Type-B.

Fig. 7: Measured (dashed) and simulated (solid) $V_{DS}$, $I_D$, and $T_j$ waveforms during short-circuit conditions for a 1200 V, 42 A 4H-SiC MOSFET at initial temperature of 25 °C for $V_{GS} = 15$, 17 and 19 V and $V_{DS} = 300$ V.

Fig. 8: Measured (dashed) and simulated (solid) $V_{DS}$, $I_D$, and $T_j$ waveforms during short-circuit conditions for a 1200 V, 31.6 A 4H-SiC MOSFET at initial temperature of 25 °C for $V_{GS} = 15$, 17 and 19 V and $V_{DS} = 300$ V.

Fig. 9: Measured (dashed) and simulated (solid) $V_{DS}$, $I_D$, and $T_j$ waveforms during short-circuit conditions for a 1200 V, 42 A 4H-SiC MOSFET at initial temperature of 25 °C for $V_{GS} = 15$, 17 and 19 V and $V_{DS} = 400$ V.

Fig. 10: Measured (dashed) and simulated (solid) $V_{DS}$, $I_D$, and $T_j$ waveforms during short-circuit conditions for a 1200 V, 31.6 A 4H-SiC MOSFET at initial temperature of 25 °C for $V_{GS} = 15$, 17 and 19 V and $V_{DS} = 400$ V.
IV. CONCLUSIONS

This paper presents modifications to the Hefner power MOSFET model and parameter extraction sequence needed to extend the model to the high-current, high-temperature conditions of short-circuit events. The simulation results for two types of commercially available SiC power MOSFETs (Types A: 1200 V, 42 A and Type B: 1200 V, 31.6 A) show good agreement with measured drain current waveforms and failure times for a wide range of $V_{GS}$ and $V_{DS}$. The electro-thermal model and simulations are used to analyze short-circuit SOA including $t_{failure}$ and $T_{j}$. On average, the failure temperature is approximately 650 $^\circ$C ± 100 $^\circ$C (near the melting temperature of the Aluminum adjacent to the peak junction temperature), and increases slightly with gate voltage for both Type-A and Type-B devices. The results of the work also indicate that a simple numerical equation can be used to represent the short-circuit SOA versus different values of $V_{GS}$ and $V_{DS}$ using the short-circuit figure of merit value $M_{SC}$. Minimizing the channel length modulation parameter $\lambda$ also improves the short-circuit SOA.

REFERENCES