A Natural ZVS High-power Bi-directional dc - dc Converter with Minimum Number of Devices

Hui Li
Tyco Electronics
Power Systems

Fang Z. Peng
Dept. of ECE
Michigan State University

Jack S. Lawler
Dept. of ECE
The University of Tennessee

Abstract – This paper introduces a new bi-directional, isolated dc-to-dc converter. A typical application for this converter can be found in the auxiliary power supply of hybrid electric vehicles. A dual half-bridge topology has been developed to implement the required power rating using the minimum number of devices. Unified zero-voltage-switching was achieved in either direction of power flow with neither a voltage-clamping circuit nor extra switching devices and resonant components. All these new features allow high power density, efficient power conversion and compact packaging. Complete descriptions of operating principle and design guidelines are provided in this paper. An extended state-space averaged model is developed to predict large and small signal characteristics of the converter in both directions of power flow. A 1.6 kW prototype has been built and successfully tested under full power. The experimental results of the converter’s steady-state operation confirm the soft-switching operation, simulation analysis, and the developed averaged model. The proposed converter is a good alternative to full-bridge isolated bi-directional dc-dc converter in high power applications.

I. INTRODUCTION

The necessity of high power isolated bi-directional dc-dc converters can be stressed in wide applications from uninterrupted power supplies, battery charging and discharging system, to auxiliary power supplies for hybrid electrical vehicles. However, most of the existing dc-dc converter topologies are of low power [1] or unidirectional [2], and cannot meet the requirements of the above applications.

Recently, some high power dc-dc converters with soft-switching operation and isolated bi-directional operation have been introduced in the literature [3]-[6]. These converters are regarded as expected candidates for such applications because they have the advantages of reduced switching losses, improved EMI and increased efficiency. However, these converters are not appropriate to achieve high power density, high reliability and low cost because of extra devices and/or complicated control circuitry resulting in bulky and costly implementation.

This paper introduces a new bi-directional, isolated dc-to-dc converter for high power applications. A dual half-bridge topology is developed to achieve higher power rating. In addition, unified zero-voltage-switching (ZVS) is possible in either direction of power flow without using voltage-clamping circuit or extra switching devices and resonant components. Therefore, only the minimum number of devices is required in the proposed topology. Like ZVS phase-shifted full bridge topologies, the proposed converter has achieved a natural ZVS by only defining the dead time of gate signals. All these features allow efficient power conversion, high power density, low cost, easy control and compacted packaging. In this paper, the operation of the proposed converter is explained and analyzed. An averaged model is developed and design guidelines are given to select the components of the converter. A 1.6 kW prototype of the converter has been built and successfully tested under full power. The experimental results of the converter’s steady-state operation confirm the simulation analysis and the averaged model. The proposed converter is a good alternative to the full-bridge isolated bi-directional dc-to-dc converter in high power applications.

II. CIRCUIT DESCRIPTION AND OPERATION PRINCIPLES

A. Circuit Description

The proposed bi-directional dc-dc converter is shown in Fig. 1. This circuit is operated with dual half-bridges placed on each side of the isolation transformer. When power flows from the low-voltage (LV) side to the high-voltage (HV) side, the circuit works in boost mode to power the HV-side load; otherwise, it works in buck mode to recharge the LV-side battery. A dual half-bridge topology is used instead of a dual full-bridge configuration for the following reasons:

1) The total device rating is the same for the dual-half bridge topology and the dual-full bridge at the same output power.

2) Although the devices of the LV side are subject to twice the de input voltage, this is not a serious concern because the dc-input voltage in the anticipated application is 12 V.

3) The dual-half bridge topology uses only half as many devices as the full-bridge topology.

B. Principles of Operation

The primary-referred equivalent circuit is shown in Fig. 2. The interval $t_0$ to $t_{12}$ of Fig. 3 describes the various stages of operation during one switching period in boost mode. One complete switching cycle is divided into thirteen steps. Each step is described briefly below. Commutation procedure in buck mode can be analogously inferred.

Step 1 (before $t_1$): Circuit steady state. S1 and D3 are conducting.

Step 2 ($t_1$ to $t_2$): At $t_1$, S1 is turned off. Cr1, Cr2 and T begin to resonate, making $V_{G3}$ fall from $V_1+V_2$. $V_i$ also drops from $V_i$. The rate of change depends on the magnitude of $I_{ref}$ which is the...
Commutation in the proposed circuit is similar to the diode-to-switch commutation mode of the Auxiliary Resonant Commutated Pole Converter (APCP) converter [7], i.e., turn-off of the main conducting device diverts the current to the corresponding snubber capacitors to charge one and discharge another, resulting in a zero voltage turn-off. The zero voltage turn-on is achieved by gating on the incoming device while the anti-parallel diode is conducting. However, unlike ARCP converter, the proposed circuit does not require an auxiliary circuit to achieve soft switching. From Fig. 2, it is clear that the conditions of soft switching in boost mode depend on the magnitude of \( I_{r1} \) and \( I_{d1} \) at \( t_r, t_1, t_2 \) and \( t_{11} \), respectively. This is summarized in equation (1). The soft-switching conditions in buck mode can also be derived similarly.

\[
\begin{align*}
I_{r1}(t_r) &> I_{d1}(t_1) \\
I_{r1}(t_1) &< 0 \\
I_{r1}(t_2) &< I_{d1}(t_7) \\
I_{r1}(t_{11}) &> 0
\end{align*}
\] (1)

III. STEADY STATE ANALYSIS

A. Output characteristics

The analysis of output characteristics is based on the primary-referenced equivalent circuit in Fig. 2 and the idealized waveforms in Fig. 4. The transferred power can be found to be:

\[
P_o = \frac{T_s}{T} \left[ \int_0^{T} I_{in} V_{r1} dt \right] = \frac{1}{D} \int_0^{\frac{1}{2} \pi} \left( \frac{4}{D} \phi_1 - \frac{4}{D} \phi_2 \right) V_{in}^2 dt
\] (2)

\( T_s \) is the period of the switching frequency and \( D = \frac{\phi_2}{2\pi} \). The output power (output voltage) can be regulated by phase shift angle \( \phi_2 \), duty cycle \( D \) and switching frequency \( f_2 \). If \( D = 50\% \) is assumed and the switching frequency is set at 20 kHz, then the output power equation can be simplified further as

\[
P_o = \frac{V_{in}^2}{\delta L_s} \frac{\phi_1 (\pi - \phi_1)}{\pi}
\] (3)

B. Design Equations

According to equation (3), when duty cycle and switching frequency are fixed, the output power is related to phase shift angle \( \phi_2 \) and leakage inductance of transformer. Fig. 5 illustrates the output power curves of \( L_s = 0.6 \mu H \) and \( L_s = 0.3 \mu H \). It is interesting to notice that if the leakage inductance is selected differently, the phase shift angle of the same output power is changed. The smaller leakage inductance results in the smaller the phase shift angle. Therefore, the leakage inductance of the transformer can be designed according to the expected phase shift angle at the required power rating.

Assume the maximum output power is \( P_o \). the input dc voltage is \( V_{in} \), the switching frequency is \( f_2 \), the expected phase shift angle at \( P_o \) is \( \phi_1 \), \( L_s \) can be calculated as follows.

\[
L_s = \frac{V_{in}^2}{P_o} \frac{\phi_1 (\pi - \phi_1)}{\pi}
\] (4)

Referred to Fig. 4, the initial states \( I_{r1}(0), I_{r1}(\phi_1), I_{r1}(\phi_2), I_{r1}(\phi_2 + \phi_1) \) of current \( I_{r1} \) during one complete switching cycle can be derived based on the boundary conditions:

\[
\begin{align*}
I_{r1}(0) &= -I_{r1}(\phi_2) \\
I_{r1}(\phi_1) &= -I_{r1}(\phi_2 + \phi_1)
\end{align*}
\] (5)
currents are calculated as:
\[ I_{\text{off}} \left|_{\text{min}} \right. \leq \frac{dv}{dt} \leq I_{\text{off}} \left|_{\text{max}} \right. \]

If \( \Delta I \) of \( I_d \) is selected as 12A, then \( I_{\text{off}} \) is designed to be
\[ I_{\text{dc}} = \frac{V_o - \Delta I}{\Delta I} \]

Finally, the soft switching condition will be verified in equation (11).
\[
\begin{align*}
I_{r2}(0) &> 0 & I_{r2}(\pi) &< 0 \\
I_{r2}(\pi + \phi) &< 0 & I_{r2}(\pi + \phi_1) &> I_{d1}
\end{align*}
\]

C. Characteristics curves

The characteristic curves are derived based on the design equations. Fig. 6 to Fig. 8 describes the system behavior when transformer leakage inductance is selected as 0.6\( \mu \)H.

Figs.6 (a)-(d) plots the input current, transformer current, \( dv/dt(\text{max}) \) and \( dv/dt(\text{min}) \) over the full output power range. The purpose of this figure is to show that the soft-switching condition is satisfied during the whole operating range. According to equation (11), soft switching is maintained at any output power in the boost mode. Soft switching of the buck mode can be similarly inferred.

Fig. 7 shows the current stress of the main switches of the low voltage side and the high voltage side against output power. The current stress of high voltage side is calculated based on the primary-referenced circuit. Fig. 8 plots the current stress as a function of phase shift \( \phi \) instead of output power.

An interesting feature can be brought to light by examining Fig. 8, which shows that the current stresses of the devices are proportional to the phase shift angle. As a result, if the phase shift is decreased for the same output power, the current stress becomes less. This is important to improve the system efficiency because the conduction loss will become the main loss for soft-switching converters.

VI. MODELING AND CONTROL SYSTEM DESIGN

In this section, the development of the averaged model and control system design is provided for the proposed converter. The traditional state-space averaging technique \[8\] and circuit-averaged approach \[9\] are difficult to be applied to the circuit. Therefore, a switching-frequency-dependent average model and a linearized small signal model has been derived to predict large and small-signal characteristics of the converter in both direction of power flow. The simulated waveforms of the average model have been compared with the detailed circuit simulation to verify the accuracy of the modeling. The experimental verifications will be illustrated in section V. The control-to-output transfer function has been generated to provide the information on the poles, zeros and the gain of the open-loop converter. The controller has been designed to stabilize the system around the nominal operating point and regulate the output voltage against the input voltage disturbance and/or load variation. The control system is simulated by Matlab/Simulink. The system transient performances are verified by the simulated model.

A. Averaged model

Assuming that duty cycle equals 50% and the switching processes are instantaneous, the primary-referenced equivalent circuit is redrawn in Fig. 9. \( I_{r1} \) and \( I_{r2} \) of Fig. 2 are redefined as \( i_t \).
the key problem of developing the average model for this
ac current flowing through the isolation transformer, the dc

and the transformer current
variables of the converter are chosen to be the inductor current
switching cycle at steady state are shown in Fig. 4. The dynamic

Fig. 6 The soft-switching conditions versus output power.

Fig. 7 The current stresses of devices versus output power.

Fig. 8 The current stresses of devices versus phase shift $\phi$.

transformer is to exclude $i_s$, which is possible because $i_s$ can be
represented by $i_s = f(v_{i2}, v_{i3}, v_f, \phi)$, using circuit analysis of the
four modes of operation. However, it is impossible to cancel $i_s$
using the ordinary state-space averaging technique. In addition,
the conventional averaging techniques are independent of
switching frequency. This will not be acceptable for the
proposed converter because the switching frequency is a possible
control variable. Thus, an extended switching-frequency-
dependent averaging technique is developed to solve these
problems. The details of the model derivation can be found in
[10] and the simplified average model in both direction of power
flow can be expressed in (12).

\[
\begin{align*}
\dot{i}_{avg} &= \frac{R_b}{L_{dc}} \dot{v}_{avg} - \frac{1}{2L_{dc}} v_{12avg} + \frac{1}{L_{dc}} v_b \\
\dot{v}_{12avg} &= \frac{1}{C_p} \dot{\dot{v}}_{avg} - \frac{2\theta_1(\pi - \phi)}{C_p T_s \cdot 2\alpha L_s} v_{34avg} \\
v_{34avg} &= \frac{2\theta_1(\pi - \phi)}{C_i T_s \cdot 2\alpha L_s} v_{12avg} + \frac{2}{C_i R_s} v_{34avg} + \frac{2}{C_i R_s} v_f 
\end{align*}
\]

where $C_f = C_s + 2C_o$.

B. Simulation and experimental verification of averaged model

The average model can be implemented and simulated using
Matlab/Simulink, which is shown in Fig. 10.

A start-up process of the open-loop converter system using a
ramp input voltage of 12 volts is simulated under the
conditions below:

$V_i = 12 V$, $R_b = 0$, $D = 50\%$, $f_s = 20$ kHz, $L_{dc} = 5 \mu H$, $L_s = 0.3 \mu H$, $C_p = C_s = 10 \mu F$, $C_o = 169 \mu F$, $V_i = 0 V$, and $R_s = 0.27$ ohms.

The waveforms for $i_s$, $v_{i2}$ (or $v_{i3} + v_f$), and $v_{34}$ (or $v_{13} + v_f$) of the
average model and detailed circuit model are shown in Fig. 11
and Fig. 12, respectively. The verification of the ac variable
simulation is demonstrated in Fig. 13. The comparison
demonstrates their similarity consistency in shape, frequency and
average magnitude.
linearized state equations can be derived as follows:

By introducing small perturbations:

\[
\begin{align*}
\tilde{v}_{in} &= V_{in} + \tilde{v}_{in}, \quad \tilde{i}_1 = \Phi_1 + \tilde{\Phi}_1, \quad \tilde{v}_{12} = V_{12} + \tilde{v}_{12}, \quad \tilde{i}_1 = I_1 + \tilde{I}_1, \\
\tilde{v}_{34} &= V_{34} + \tilde{v}_{34}, \quad \text{where } \tilde{i}_1 \text{ is a current source placed across the} \\
\text{nominal load and choosing } (\tilde{\Phi}_1, \tilde{\Phi}_2, \tilde{\Phi}_3, \tilde{\Phi}_4) \text{ as state variables,} \\
(\tilde{v}_{in}, \tilde{v}_{12}, \tilde{v}_{34}) \text{ as control inputs and } \tilde{v}_{34} \text{ as controlled output, the} \\
\text{linearized state equations can be derived as follows:}
\end{align*}
\]

\[
\begin{pmatrix}
\dot{\tilde{\Phi}}_1 \\
\dot{\tilde{\Phi}}_2 \\
\dot{\tilde{\Phi}}_3 \\
\dot{\tilde{\Phi}}_4
\end{pmatrix} =
\begin{pmatrix}
0 & -\frac{1}{2L_{in}} & 0 & 0 \\
\frac{1}{C_p} & 0 & -\frac{2\Phi_1 - 2\Phi_2}{K_1} & 0 \\
0 & \frac{2\Phi_1 - 2\Phi_2}{K_3} & \frac{-1}{C_R} & 0 \\
\end{pmatrix}
\begin{pmatrix}
\tilde{v}_{in} \\
\tilde{v}_{12} \\
\tilde{v}_{34}
\end{pmatrix} +
\begin{pmatrix}
\frac{1}{L_{dc}} \\
0 \\
0 \\
\end{pmatrix}
\begin{pmatrix}
\tilde{i}_1 \\
\tilde{i}_2 \\
\tilde{i}_3 \\
\end{pmatrix}
\]

Where \(K_1 = 2Ts_0^2LsC_p, K_3 = 2Ts_0^2LsC_o\).

Assume the nominal operating point of dc-dc converter is selected as:

\[
P_o = 1.6 kW, \quad V_{in} = 12 V, \quad \Phi_1 = 0.16\pi, \quad R_s = 0.36\Omega,
\]

\[
L_{dc} = 5 \mu H, \quad C_p = C_o = 10 mF, \quad 169 mF, \quad f_s = 20 kHz.
\]

\(L_s\) is designed as 0.3 \(\mu H\) to have smaller conduction loss at 1.6 kW. The transfer function matrix from input vector to output is calculated as follows.

\[
\begin{align*}
T_{ij}(s) &= \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} \\
&= \frac{0.319 \times 10^9}{s^3 + 15.964s^2 + 0.100 \times 10^8 s + 0.159 \times 10^9} \\
T_{il}(s) &= \frac{\tilde{v}_o(s)}{\tilde{i}_1(s)} \\
&= \frac{617.048s^2 - 0.343 \times 10^5 s + 0.617 \times 10^5}{\Phi_1(s)} \\
&= \frac{s^3 + 15.964s^2 + 0.100 \times 10^8 s + 0.159 \times 10^9}{s^3 + 15.964s^2 + 0.100 \times 10^8 s + 0.159 \times 10^9}
\end{align*}
\]

The transfer functions are used to design the controller to allow the converter to meet load regulation and transient response specifications, especially the control-to-output transfer function \(T_{il}(s)\). The root locus plot of \(T_{il}(s)\) is shown in Fig 14. The root locus of the compensated system is shown in Fig. 15, in which a controller is obtained by trial and error as shown in (15).
A 1.6 kW soft-switched bi-directional dc-dc converter has been built and experimentally tested to validate the previous analysis. The prototype is pictured in Fig. 20. In order to compare with the size of a dual full bridge converter for the similar application, the prototype is placed on a 0.375" liquid cooled heat sink with overall size of about 7.5" width and 13.5" in length. The actual usable area is 7.25" by 8.5", which shows the high power density characteristic of the proposed topology.

The experimental results and circuit simulation results of static performance in boost mode are obtained in Fig. 21. There is a good agreement between simulation results and experimental results. For inductor current \( i_L \) and transformer current \( i_T \), the wave shapes of simulation and those of experiment agree with each other. In addition, the peak values of \( i_L \) in simulation are +45 A and −55 A and those of experimental values are +40 A and −50 A. The average value of \( i_L \) in (a) is about 22 A and that of (b) is 25 A. The magnitude of \( v_{o2} \) in simulation is 26 V, the experimental magnitude is also about 26 V. In addition, there are also similarities in shape and frequency of \( v_{o2} \). The phase shift angle between \( v_{o1} \) and \( v_{o2} \) in the two figures are consistent. Although the magnitude and the shape of \( v_{o2} \) are almost the same in the two figures, the experimental result of \( v_{o2} \) waveform has a ringing effect. This is because it is hard to measure directly the two terminals of the primary side of transformer, consequently the measurement loop may be the main reason for this ringing effect. The details of the switching process of S2 and S4 in buck mode are demonstrated in Fig. 22. The voltage source of the HV side is 116 V. The load resistance of the LV side is 0.1 \( \Omega \). The phase-shift angle of S3 leading to S1 is 0.04 \( ^\circ \), namely 1 \( \mu \)s under 20 kHz switching frequency. The leakage inductance of the transformer in this prototype is measured as 0.4 \( \mu \)H. The soft switching of other devices can be derived similarly.

Figure 23 presents the output characteristics of the converter from 0 to full output power under open-loop control. As indicated in the figure, the “-” trace is the experimental result, the “o” one is of detailed circuit simulation and the “+” one is of average model simulation. The similarity of the three curves confirms the validity of the average model. The difference between the average model, detailed circuit model and prototype can be explained as follows. The average model assumes all switches and components are ideal, there are no losses in switches, capacitors, the inductor or the transformer. The detailed circuit model is a better approximation of the actual circuit. Some of the above losses have been taken into account and the efficiency will be lower than that of average model. The difference between the circuit model and the prototype is likely in the higher device losses and magnetic losses in the prototype due to the imperfect devices and transformer models in detailed circuit simulation. Therefore, the output voltage of average model is higher than that of the detailed circuit model and the detailed
Fig. 17 System response of load step change from 0.36 ohm to 0.4 ohm.

(a) $i_1$ response of load step change (from 0.36 ohm to 0.4 ohm)

(b) $v_{12}$ response of load step change (from 0.36 ohm to 0.4 ohm)

(c) $v_{12}$ response of load step change (from 0.36 ohm to 0.4 ohm)

Fig. 18 Output response of input voltage step change from 12 V to 11 V.

Fig. 19 Output response when reference voltage change from 24 V to 25 V.

(a) Simulation results of $v_r1$ (5V/div), $i_1$ (5A/div), $i_r$ (50A/div), and $v_r2$ (50 V/div)

(b) Experimental results of $v_r1$ (5V/div), $i_1$ (5A/div), $i_r$ (50A/div), and $v_r2$ (50 V/div)

Fig. 20. Photo of the prototype.

Fig. 21. Steady state operation of boost mode ($v_b = 3$ V).
VI. SUMMARY
This paper presents a new soft-switched bi-directional dc-dc converter. Compared with the other soft-switched bi-directional dc-dc converters, this new topology has the following features:

- Decreased number of devices.
- Compared with the full-bridge topologies, this converter has a half-bridge on both the LV side and the HV side, decreasing the number of devices by half.
- Unified soft-switching scheme without an auxiliary circuit.
- Unified ZVS is possible for all of the devices in either direction of power flow. Moreover, instead of using an auxiliary circuit, soft-switching conditions are ensured by Eq. (11).
- Low cost design is lightweight, compact and reliable.
- The design has less control and accessory power needs than converters for the similar applications.

In addition, a large-signal mathematical model and its linearized small-signal model are developed and verified for the proposed circuit. Moreover, a controller has been designed and the simulation results show the converter system has a satisfactory transient response against load variation and disturbed battery voltage. The averaging technique proposed in this paper also provides a possible solution to the other bi-directional dc-dc converters with a high-frequency isolation transformer. The experimental waveforms confirm the averaged model, soft-switching operation and good steady-state performance of the converter.

REFERENCES