A 40MHz-BW Two-step Open-loop VCO-based ADC with 42fJ/step FoM in 40nm CMOS

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Abstract—A two-step open-loop VCO-based ADC with 1st-order noise shaping and intrinsic nonlinearity mitigation is presented. With the open-loop structure and highly digital building blocks, a robust performance, high bandwidth and high efficiency is achieved. The nonlinearities of the VCOs in the coarse and fine quantizers are improved by a distortion cancellation and a voltage swing reduction scheme respectively. Because of the intrinsic DEM of the VCO-based quantizer output, the matching requirement of the DAC cells is greatly relaxed. The design is implemented in 40nm CMOS and shows that, with 1.6GHz sampling frequency, the two-step VCO-based ADC reaches 40MHz bandwidth, 59.5dB SNDR and 67.7dB SFDR. The power consumption is only 2.57mW, corresponding to an excellent FoM of 42fJ/step.

I. INTRODUCTION

New standards of wireline and wireless communications always require larger signal bandwidths. For example, VDSL2 and WLAN 802.11n are expected to extend their analog bandwidths to 30MHz and 40MHz respectively. In the meantime, more and more work is done with mobile devices powered by a battery, for example tablets and smart phones. In such products low power consumption is now the most important design criterion.

As technology scaling continues, one trend of ADC design is shifting more functions from the voltage and the analog domains into the time and the digital domains, by using voltage-controlled ring oscillators (VCO) or pulse-width modulators (PWM). In Fig. 1, the structure and behavioral model of a VCO-based quantizer [1] are shown. First, a ring VCO converts the input voltage into phase information, which is characterized by the rising/falling edges of the VCO outputs. Then, a sense-amplifier flip-flop (SA FF) is used to synchronize each VCO output, introducing a quantization error in the phase domain. Finally, a digital differentiator (constructed by a TSPC FF and an XOR gate) processes the sampled phase and outputs digital frequency information. By applying such a simple, highly digital circuit, not only quantization is done, but also 1st-order noise shaping is obtained. In addition, there is intrinsic dynamic element matching (DEM) for the digital output. However, the VCO nonlinear transfer function causes distortion and limits its application in ADC design. Although the 2nd-order harmonics can be cancelled by a pseudo differential topology, the VCO 3rd-order nonlinearity is still a performance limitation for designs with more than 6-bit linearity. In [1], the VCO-based quantizer is used in a 3rd-order delta-sigma loop and the VCO nonlinearity is suppressed by the preceding analog integrator. Look-up-table-based digital calibrations are used to solve the VCO nonlinearity in an open-loop DSM [2]. In [3], the analog input is first modulated by a PWM and then fed into the VCO-based quantizer. Because of the two-points nature of the PWM signal, the VCO behavior is intrinsically linear. In [4], the VCO-based quantizer is only used for residual signal conversion, and the VCO linearity is improved by its reduced input voltage swing.

In ADC design, the two-step conversion topology [5] has been proposed to break the exponential increase of the number of comparators in flash ADCs, at the expense of finishing one conversion in two clock periods. A digital-to-analog converter (DAC) and a subtractor with full accuracy are required to generate the residual signal.

In our proposed ADC design, we combine the two-step conversion principle with a VCO-based quantizer to achieve 1st-order noise shaping and solve the VCO nonlinearity issue. At the same time, the intrinsic DEM of the VCO-based quantizer output relaxes the DAC matching requirement greatly. By applying the proposed architecture, a 40MHz-BW ADC with excellent 42fJ/step figure-of-merit (FoM) is realized. The paper is organized as follows. Section 2 introduces the proposed two-step VCO-based ADC architecture. The circuit designs of the VCO-based quantizer, and the DAC together with the subtractor are described in section 3. The measurement results are presented and discussed in section 4. Finally, section 5 draws conclusions.

Figure 1. Structure and behavioral model of the VCO-based quantizer [1].
II. PROPOSED TWO-STEP OPEN-LOOP VCO-BASED ADC ARCHITECTURE

A. Intrinsic Nonlinearity Mitigation of VCO-based Quantizer

The proposed two-step VCO-based ADC architecture and its illustrative signal spectrums are shown in Fig. 2 (details of the VCO-based quantizers are presented in Fig. 1). Its structure and operation principle are similar to a two-step flash ADC [5] except for two differences. First, highly digital VCO-based quantizers with 1st-order noise shaping and intrinsic DEM are used instead of simple flash quantizers. Secondly, there is no analog amplifier preceding the fine quantizer. Hence, the power consumption is very low.

In our proposed architecture, the differential N-bit VCO-based coarse quantizer converts the analog input into digital bits. With full voltage swing input, the coarse output includes not only the signal, but also 1st-order noise shaped quantization error and distortions. Then, by applying an N-bit DAC and a subtractor, the residual error of the coarse quantizer is obtained. If the coarse quantization step is small enough and without amplifier, the voltage swing of the residual signal is much smaller than the ADC input signal swing. Since the subtractor is linear, the noise and distortion of the residual signal are almost the same as those of the coarse output. The residual error is processed further by the M-bit fine VCO-based quantizer. With the low input signal swing, the transfer function of the fine VCO-based quantizer can be considered very linear. In the fine quantizer, although the input signal swing is small, because of the VCO integration and the time-domain quantization, all $2^{M-1}$ quantization steps are used [6] and small quantization error is introduced. Finally, the digital outputs of the coarse and fine quantizers are summed as the output of the whole ADC.

In this design, the gain of path 2 in Fig. 2 (the DAC, the subtractor and the fine VCO-based quantizer) is designed to be 1 to match that of the path 1. By doing this, all nonidealities (quantization error, thermal noise, distortion) of the coarse VCO-based quantizer are cancelled, and the open-loop two-step ADC is equivalent to a linear 1st-order Delta-Sigma modulator (DSM) with M-bit quantization. The noise contributions of the DAC and the VCO in the fine quantizer refer to the ADC input directly, and they have been optimized in circuit-level design.

B. Intrinsic Dynamic Element Matching for DAC

In the VCO-based quantizer, the different phase outputs of the ring VCO change their status consecutively, which means that there is an intrinsic DEM on the quantizer digital outputs. For the DAC design, because of the intrinsic DEM of the digital input, the DAC cell matching requirement (for example, about 8% standard deviation for 10-bit linearity) can easily be achieved and is not the bottleneck for the overall ADC linearity.

III. CIRCUIT IMPLEMENTATION OF TWO-STEP OPEN-LOOP VCO-BASED ADC

To verify the proposed two-step open-loop VCO-based ADC architecture, a 40MHz-BW 10-bit ADC has been designed. In this design, both the coarse and fine VCO-based quantizers are 5-bit pseudo differential structures (composed of 2 4-bit single-ended ones). The sampling frequency of the two-step VCO-based ADC is 1.6GHz, with an oversampling ratio (OSR) of 20 for a 40MHz bandwidth.

A. VCO-based Quantizer Design

The schematic of the 15-stage ring VCO of a 4-bit single-ended quantizer is presented in Fig. 3; the delay cell circuit is shown in the blue dashed box. The oscillation frequency of the VCO is controlled by the drain currents of the delay cells, which is generated by the voltage-controlled current source. To accommodate the process variation during circuit fabrication, a 3-bit binary control scheme is adopted to tune the transconductance of the current source, and so the VCO
With a 500mV common-mode voltage and a 400mVpp input swing, the maximum oscillation frequency of the ring VCO is designed to be no larger than half of the sampling frequency (800MHz) to avoid overloading the quantizer in the time domain.

Transistor-level simulations show that with 0dBFS input, the signal-to-noise-distortion ratio (SNDR) of the 5-bit pseudo differential VCO-based quantizer is about 37dB. When the input is reduced to -22dBFS, the VCO-based quantizer is quite linear, with around -76dBFS 3rd-order distortion. The simulated phase noise of the VCO is about -113dB/Hz at 10MHz offset frequency; the calculated signal-to-phase-noise-ratio is about 68dB according to the formula in [7]. It is clear that this circuit noise does not limit the ADC performance.

B. DAC and Subtractor Design

The DAC used in the two-step VCO-based ADC is a current-steering DAC. Its schematic (together with the subtractor) is shown in Fig. 4. The basic DAC cell is composed of a current source transistor, a cascode transistor and a pair of switches with full swing input. For the current source transistor, about 0.64µm² area is chosen in the design to achieve the required matching. For the cascode transistor, 2x the minimum gate length is used to provide efficient shielding from the switching node to the quiet bias node and to increase the DAC output impedance. Even with full swing DAC input, the switch transistor is still in the saturation region, increasing the DAC output impedance further.

To avoid active power consumption, a passive subtractor is applied in this design, by connecting resistors (500Ω) between the ADC inputs and the DAC outputs. The output currents of the current-steering DAC flow through the resistors and cause corresponding voltage drops across the resistors. The ADC differential input voltage minus the voltage drop results in the residual signal for the fine VCO-based quantizer. Noise simulations show that the RMS (root-mean-square) output noise voltage of the current-steering DAC and the subtractor is about 54µV, which corresponds to about -77dBFS.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed two-step open-loop VCO-based ADC has been fabricated in 40nm CMOS. The die photo is given in Fig. 5, with only 0.017mm² core area. To illustrate the two-step conversion idea, both the digital outputs of the coarse and the fine VCO-based quantizers are converted into binary codes and fed to digital buffers and low-voltage differential signal (LVDS) interface. The other area is occupied by on-chip decoupling capacitors for power supply and bias.

The measured results of the two-step VCO-based ADC with 12MHz, -1dBFS input signal are shown in Fig. 6. In the top of Fig. 6, the power spectral density (PSD) of the coarse quantizer output is plotted. With this large input swing and the nonlinear VCO transfer function, the 3rd-order distortion appears, and the linearity of the quantizer is about 5-bit. With limited matching of the pseudo differential quantizer, part of the 2nd-order distortion also still remains. In the middle of Fig. 6, the PSD plot of the fine quantizer output is shown.
Here the signal is about 20dB less than that of the coarse quantizer output, and the distortions are almost the same. For such a small input signal swing, the fine VCO-based quantizer is very linear, and the distortions in the fine quantizer output originate from the residual signal. By adding the coarse and fine quantizer outputs together, their distortions cancel each other. As a result, 59.5dB SNDR and 67.6dB spurious-free dynamic range (SFDR) are achieved for the whole ADC. The power consumption of the two-step VCO-based ADC is 2.57mW, most of which is from the digital gates (FF, XOR). Because of the simple architecture and the highly digital building blocks, an excellent FoM ($P/(2*BW*2^{ENOB})$) of 42fJ/step is achieved. The performance of the two-step open-loop VCO-based ADC is summarized and compared to the state-of-the-art in table 1. Our design improves the FoM almost 2× compared to the state-of-the-art in high-bandwidth (>20MHz) DSMs.

![Figure 6](image)

Figure 6. Measured results of the two-step 1st-order VCO-based DSM with -1dBFS 12MHz sine input. Top: PSD plot of the coarse quantizer output; Middle: PSD plot of the fine quantizer output; Bottom: PSD plot of the overall ADC output.

V. CONCLUSIONS

An open-loop two-step VCO-based ADC architecture is proposed to realize 1st-order noise shaping and solve the VCO nonlinearity issue. The DAC matching is greatly relaxed as its input has intrinsic DEM. Because of the open-loop and highly digital structure, a high bandwidth low power consumption and small area can easily be achieved. Measurement results show that a 40MHz-BW ADC in 40nm CMOS achieves an SNDR of 59.5dB and an SFDR of 67dB with 1.6GHz sampling frequency and only 2.57mW power consumption. The excellent FoM is only 42fJ/step.

### Table I

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REFERENCES


