A Component-Minimized Dual-Output Multilevel Converter and Its Applications

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Abstract—In this paper, a component-minimized dual-output multilevel converter is proposed. The operating principle and constraints on voltage and frequency of the dual outputs are detailed. Three applications of the proposed converter are explained: a) online uninterruptible power supplies (UPSs), b) six-phase wind generators, and c) doubly fed induction generator (DFIG) wind power systems. Also, limits on the modulation index in each application are analyzed. Furthermore, the loss breakdown of the online UPS system is analyzed and compared with a conventional back-to-back converter. The simulation results are included in the summary to verify the validity of the proposed topology.

I. INTRODUCTION

A dual-output DC/AC converter is used in the following industrial applications: dual 3-phase motor drives, online UPS systems with two controllable terminals, and six-phase motor drives [1]-[3]. In a conventional system, a separate converter is used for each output powered from the same dc-link voltage. This results in increased component count and adds to the inverter cost. Previous research has explored component-minimized topologies which reduce the number of semiconductor switches and associated drivers. Two reduced switch scenarios are proposed in [2] and [3], where the converters called “B4” and five-leg converters are presented, respectively (see Fig. 1). In the first case of the B4 converter, one output phase is connected to the midpoint of the dc-bus instead of the converter leg as shown in Fig. 1(a). In the second case of the five-leg converter, two ac ports share one leg, shown in Fig. 1(b). In [4], the combined use of dc midpoint connection and phase leg sharing has been proposed, which is called four-leg converter as shown in Fig. 1(c). Moreover, a similar approach is applied in single phase system and three-phase four-wire system [5]. The nine-switch converter is a recent and interesting solution [6]-[7], shown in Fig. 1(d). Moreover, the synthesis of nine-switch and dc-midpoint connection is called the six-switch converter [8], where one switching leg is replaced with dc-bus capacitors as shown in Fig. 1(e). This approach is also employed in single phase system, called three-switch converter. However, the variant form is achieved at the expense of dc bus utilization and output waveform quality [9]-[10].

![Fig. 1. Review of topology with reduced switches](image)

It is noted that the nine-switch converter still has two-level converter drawbacks, such as low efficiency, poor THD, high EMI, etc. Nowadays, the multilevel converters, especially three-level converters, are a promising alternative to the conventional two-level converters, due to their ability to meet the increasing demand of power ratings and power quality with lower THD, lower EMI, and higher efficiency [11]-[12]. Reference [13] applied new IGBT modules in advanced Neutral-Point Clamped (NPC) 3-level converters to achieve higher efficiency. The active NPC (ANPC) inverter is proposed to overcome the unequal power loss distribution among the devices [14]. This paper proposes a component-minimized dual-output multilevel converter which synthesizes the aforementioned three-level topology.
and nine-switch topology. The proposed converter retains most of the desirable features of multilevel converter such as lower THD, low EMI. More advantages are as follow:

1. More economical; reduced in size and weight. As for proposed T-type variant converter (see Fig. 2(b)), the switch count is reduced by 12.5% in comparison to two separate converters.

2. High dc bus utilization. In case of dual outputs at same frequency and same phase, there is no reduction compared to conventional separate converters, which will be discussed in section III.

3. Higher efficiency. For instance, in online UPS application, due to the effect of dual-current cancellation, the total conduction loss will be greatly reduced, which will be explained in section IV.

II. PROPOSED DUAL-OUTPUT MULTILEVEL CONVERTER TOPOLOGY AND MODULATION SCHEME

A. Proposed Topology

Fig. 2(b) shows the proposed three-phase switch-minimized dual-output 3-level converter topology. It is noted that the middle switch (\(S_{AM}, S_{BM}, S_{CM}\)) in each individual leg is shared by the top and bottom converters, thereby reducing the switch count by 12.5% in comparison to the traditional dual separate converters (see Fig. 2(a)).

B. Modulation Scheme and Constraint

The reduction of switch number in the proposed converter topology imposes certain constraints on the switching state design. Due to the middle switches shared by both of top and bottom sets, the proposed converter has only 6 valid switching states per phase as listed in TABLE I. It is noted that 3 switching states are forbidden, where the bottom output \(V_{x2}\) is greater than the top one \(V_{x1}\). For instance, when the top set output is \(-V_{dc}/2\) and the bottom one is \(+V_{dc}/2\), the \(S_{xT}, S_{xM}\) and \(S_{xB}\) should be conducted simultaneously, yielding a short-though loop. Consequently, this switching state cannot be achieved.

TABLE I. SWITCHING STATES IN T-TYPE VARIANT 3-LEVEL CONVERTER \((X=A, B \text{ OR } C)\)

<table>
<thead>
<tr>
<th>STATES</th>
<th>(S_{xT})</th>
<th>(S_{xM})</th>
<th>(S_{xB})</th>
<th>(S_{xZ1})</th>
<th>(S_{xZ2})</th>
<th>(V_{x1})</th>
<th>(V_{x2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>VALID</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<td>0</td>
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<td></td>
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<td>1</td>
<td>0</td>
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<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(V_{dc}/2)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-(V_{dc}/2)</td>
<td>(V_{dc}/2)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>-(V_{dc}/2)</td>
<td>(V_{dc}/2)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-(V_{dc}/2)</td>
<td>(V_{dc}/2)</td>
</tr>
</tbody>
</table>

Fig. 3 shows the generalized carrier-based modulation scheme for the proposed dual-output converter. As shown in Fig. 3, these two modulating waveforms are compared with a common triangular carrier. It can be observed that the forbidden states occur when the bottom reference is greater than the top one. Therefore, in order to avoid forbidden states occurring, it is significant to guarantee that the reference of the top set should be greater than that of the bottom at any instant. This fact becomes the main constraint for the switching scheme design of proposed converter.

From valid switching states in Table I, it can be seen that the state of \(S_{AM}\) is high only when the states of \(S_{xZ2}\) and \(S_{xZ3}\) are different. Therefore, in the normal situation \((V_{Top, ref}>V_{Bot, ref})\), the switching behavior of \(S_{AM}\) can be obtained from (1).

\[
S_{AM} = \overline{S_{xZ2}} + \overline{S_{xZ3}}
\]  

In term of the rest of switches, the switching pattern is the same as that in the traditional dual separate converters. Taking the top set as an example, as shown in Fig. 3, when the top set reference is at the positive cycle, \(S_{xT}\) is constantly high. Meanwhile, if the top reference is higher than the carrier, \(S_{xT}\) is “1” and \(S_{xZ}\) is “0”, which yields the high-level
output. In contrast, if the top reference is lower than the carrier, \( S_{ref} \) is high and \( S_{ref} \) is low, resulting in the zero-level output.

Fig. 3. Modulation Scheme and Constraint of Proposed Converter

III. MODULATION INDEX ANALYSIS

According to the operating frequency and phase difference between two outputs, the proposed converter can be operated in the following three modes.

- **MODE 1:** Same Frequency and Same Phase (SFSP). In this mode, the two outputs are at same frequency and same phase. Therefore, it is particular suitable for the online UPS application shown in Fig. 4 (a), where the voltage of the load is forced to follow that of the grid [7].

- **MODE 2:** Same Frequency and Different Phase (SFDP). It can be applied in six-phase large-scale wind generation in Fig. 4 (b), where the phase of one output is shifted by 30° or 60° with respect to the other [15].

- **MODE 3:** Different Frequency (DF). This can be operated in DFIG wind generation in Fig. 4 (c) or some dual-motor drive application [16].

A. CASE 1: Same Frequency and Same Phase

In order to maximum the modulation index and avoid intersecting each other, the reference signals of the top set are upward to the top of the dc plane, whereas the bottom set references are pushed to the bottom by adding appropriate dc bias. The references of two sets \((v_{Top}, v_{Bot})\) are as follows:

\[
\begin{align*}
v_{Top}(t) &= M_{Top} \sin(\omega t) + (1 - M_{Top}) \\
v_{Bot}(t) &= M_{Bot} \sin(\omega t) - (1 - M_{Bot})
\end{align*}
\]

(2)

where \( M_{Top} \) and \( M_{Bot} \) are the modulation indices of top set and bottom set (defined as the peak-to-peak magnitude of the sinusoid reference divided by the peak-to-peak magnitude of the carrier), respectively.

The constraint that the top reference should be greater than the bottom one should be satisfied as shown in (3) [7] [10].

\[
M_{Top} \sin(\omega t) + (1 - M_{Top}) \geq M_{Bot} \sin(\omega t) - (1 - M_{Bot})
\]

(3)

From (3), we can get (4).

\[
M_{Bot} \leq 1 \leq M_{Top} + \frac{2 - 2 \times M_{Top}}{1 + \sin(\omega t)}
\]

(4)

From (4), we can see that \( M_{Top} \) and \( M_{Bot} \) can approach 1 simultaneously. Fig. 5 illustrates the modulation waveforms at different modulation indices (0~1). It can be observed that both of modulation indices can simultaneously reach
the maximum of unity, which means the proposed converter can output the same voltage as traditional back-to-back topology.

For SFDP operation with phase difference $\theta$, the reference voltages and modulation constraints are as follows:

\[
\begin{align*}
\tilde{v}_{\text{top}}(t) &= M_{\text{top}} \sin(\omega t + \theta) + (1 - M_{\text{top}}) \\
\tilde{v}_{\text{bot}}(t) &= M_{\text{bot}} \sin(\omega t) - (1 - M_{\text{bot}})
\end{align*}
\]

(5)

\[
M_{\text{top}} \sin(\omega t + \theta) + (1 - M_{\text{top}}) \geq M_{\text{bot}} \sin(\omega t) - (1 - M_{\text{bot}})
\]

(6)

Assuming that $M_{\text{top}} = M_{\text{bot}} = M$, (6) can be simplified to (7).

\[
M \leq \frac{2}{2 - 2 \cos(\theta) \sin\left(\frac{\theta}{2}\right)}
\]

(7)

The maximum modulation index $M_{\text{max}}$ can be obtained expressed as (8), and is depicted in Fig. 6.

\[
M_{\text{max}} = \frac{1}{1 + \sin\left(\frac{\theta}{2}\right)}
\]

(8)

Fig. 6. The maximum modulation index with phase angle

It is observed that $M_{\text{max}}$ is decreased with the increase of the absolute value of the phase difference. In the worst case, the modulation index is reduced to one half, which means that the dc bus voltage should be doubled in order to maintain the same output voltage as that in traditional topology.

C. CASE 3: Different Frequency

Assuming that the modulation references are at different frequency and phase angle, the reference voltages and modulation constraint are as follows:

\[
\begin{align*}
\tilde{v}_{\text{top}}(t) &= M_{\text{top}} \sin(\omega t + \theta) + (1 - M_{\text{top}}) \\
\tilde{v}_{\text{bot}}(t) &= M_{\text{bot}} \sin(\omega t) - (1 - M_{\text{bot}})
\end{align*}
\]

(9)

\[
M_{\text{top}} \sin(\omega t + \theta) + (1 - M_{\text{top}}) \geq M_{\text{bot}} \sin(\omega t) - (1 - M_{\text{bot}})
\]

(10)

From (10), we can obtain (11), which shows that the sum of two modulation indices must not exceed 1.

\[
M_{\text{bot}} + M_{\text{top}} \leq 1
\]

(11)

Fig. 7 illustrates the two examples where two outputs are operated at different frequencies. It is noted that the modulation indices $M_{\text{bot}} = M_{\text{top}} = 0.5$ are critical values. Therefore, the dc voltage of the converter has to be twice as high as the rated dc voltage of traditional topologies with the same ac outputs.
IV. Efficiency Comparison of Online UPS System

In order to effectively inspect efficiency of the proposed dual-output topologies, a case study of a 30kW online UPS is taken as an example (see Fig. 3 (a)). It is worth mentioning that, due to the distinctive topological structure of proposed topology, input-output currents flowing paths are coupled. Besides, the system efficiency is dependent on a series of variables such as output power, load power factor, modulation index, and switching frequency, which makes the efficiency analysis complicated.

Assuming that the voltage and current of two sets are shown Fig. 8, it can be divided into 9 sections in one power cycle based on the directions of voltages and currents.

Basically, the 9 sections can be divided into one category, while the current paths in the second one are coupled (e.g., (3), (4), etc.). Hence, the following analysis only chooses (2) and (4) as examples.

Interval (2): Fig. 9 illustrates the operating process in one switching cycle. Since the top and bottom current paths are decoupled, the loss calculation in this process is the same as that for traditional back-to-back converter.

As shown in Fig. 9, the top current \(i_{\text{Top}}\) commutes between \(S_{Z1}\) and \(D_T\), whereas the bottom current \(i_{\text{Bot}}\) commutes between \(S_{Z2}\) and \(D_B\). Equation (12) shows the switching loss in this interval, including the turn-on losses of \(S_{Z1}\) and \(S_{Z2}\) (\(E_{\text{on}S_{Z1}}\) and \(E_{\text{on}S_{Z2}}\)), turn-off losses of \(S_{Z1}\) and \(S_{Z2}\) (\(E_{\text{off}S_{Z1}}\) and \(E_{\text{off}S_{Z2}}\)), the reverse recovery losses of \(D_B\) and \(D_T\) (\(E_{\text{on}D_T}\) and \(E_{\text{on}D_B}\)).

\[
E_{\text{sw}, z} = \sum_{n=0}^{N} E_{\text{on}S_{Z1}} [i_{\text{Top}}(n)] + \sum_{n=0}^{N} E_{\text{on}S_{Z2}} [i_{\text{Top}}(n)] + \sum_{n=0}^{N} E_{\text{off}S_{Z1}} [i_{\text{Top}}(n)] + \sum_{n=0}^{N} E_{\text{off}S_{Z2}} [i_{\text{Top}}(n)]
\]

\[
E_{\text{sw}, z} = \sum_{n=0}^{N} E_{\text{on}D_B} [i_{\text{Bot}}(n)] + \sum_{n=0}^{N} E_{\text{on}D_T} [i_{\text{Bot}}(n)] + \sum_{n=0}^{N} E_{\text{off}D_B} [i_{\text{Bot}}(n)]
\]

Interval (4): Fig. 10 illustrates the working process of this interval. It is noted that the current flowing paths of two sets are coupled.

For the conduction loss, it is noted that the current flowing through \(S_T\) is the sum of \(i_{\text{Top}}\) and \(i_{\text{Bot}}\) when the converter is operated in state 3. From Fig. 8, we can see the current sum \(i_{\text{Sum}}\) is less than either of \(i_{\text{Top}}\) or \(i_{\text{Bot}}\) due to the partial cancellation of two currents, which means the conduction loss can be reduced greatly compared to the traditional back-to-back converter. Furthermore, whether the IGBT \(S_T\) or the anti-parallel diode \(D_T\) is conducted in state 3 depends on the polarity of the sum current \(i_{\text{Sum}}\). If \(i_{\text{Sum}}\) is positive, \(S_T\) will be conducted, while the anti-parallel diode \(D_T\) will be conducted when the \(i_{\text{Sum}}\) is negative.
The conduction loss in this switching cycle is presented in (13)-(14).

\[
E_{\text{con}+\Delta} = \sum_{n=0}^{N_1} v_{D_T} [i_{\text{Top}}(n)] \cdot i_{\text{Top}}(n) \cdot (d_{\text{Top}} - d_{\text{Bot}}) T_s + \sum_{n=0}^{N_2} v_{S_T} [i_{\text{Sum}}(n)] \cdot i_{\text{Sum}}(n) \cdot d_{\text{Bot}} + v_{S_T} [i_{\text{Bot}}(n)] \cdot i_{\text{Bot}}(n) \cdot d_{\text{Bot}} \tag{13}
\]

\[
E_{\text{con}+\Delta} = \sum_{n=0}^{N_3} v_{D_T} [i_{\text{Top}}(n)] + v_{S_T} [i_{\text{Top}}(n)] \cdot i_{\text{Top}}(n) \cdot (1 - d_{\text{Top}}) T_s + \sum_{n=0}^{N_4} v_{D_T} [i_{\text{Bot}}(n)] + v_{S_T} [i_{\text{Bot}}(n)] \cdot i_{\text{Bot}}(n) \cdot (1 - d_{\text{Bot}}) T_s \tag{14}
\]

where \(E_{\text{con}+\Delta}\) is the conduction losses when output level is high, \(E_{\text{con}+\Delta}\) is the conduction losses when output level is zero.

For the top set, the switching loss occurs in the commutation process between states 1 and state 2, including the turn-on losses of \(S_{11}(E_{\text{on}S_{11}})\), turn-off losses of \(S_{11}(E_{\text{off}S_{11}})\), and the reverse recovery losses of \(D_T(E_{\text{off}D_T})\). For the bottom set, the switching loss occurs in the commutation process between states 2 and state 3, including the turn-on losses of \(S_{M}(E_{\text{on}S_M})\), turn-off losses of \(S_M(E_{\text{off}S_M})\), and the reverse recovery losses of \(D_{Z3}(E_{\text{off}D_{Z3}})\). The switching loss in this interval \(E_{\text{sw}}\) can be expressed as follows.

\[
E_{\text{sw}} = \sum_{n=0}^{N_3} E_{\text{on}S_{11}} [i_{\text{Top}}(n)] + \sum_{n=0}^{N_4} E_{\text{off}S_{11}} [i_{\text{Top}}(n)] + \sum_{n=0}^{N_4} E_{\text{off}D_T} [i_{\text{Top}}(n)] + \sum_{n=0}^{N_4} E_{\text{off}S_{M}} [i_{\text{Bot}}(n)] + \sum_{n=0}^{N_4} E_{\text{off}D_{Z3}} [i_{\text{Bot}}(n)] \tag{15}
\]

The calculation parameters are listed in TABLE II. The analytic results are shown in Fig. 11.

<table>
<thead>
<tr>
<th>TABLE II. PARAMETER FOR A 30kW ONLINE UPS SYSTEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Items/Output Voltage</td>
</tr>
<tr>
<td>Input/Output Voltage</td>
</tr>
<tr>
<td>DC-bus Voltage</td>
</tr>
<tr>
<td>Filter Inductor</td>
</tr>
<tr>
<td>Filter Capacitor</td>
</tr>
</tbody>
</table>

Fig. 11(a) shows the loss breakdown of the proposed converter when it is operated at output power 30kW (resistive load), unity input power factor, a switching frequency of 10 kHz, and the inverter modulation index of 0.89. It can be seen that the conduction losses are reduced and, correspondingly, efficiency is higher in the proposed converter compared to traditional back-to-back 3-level (B2B 3L) topology. In contrast, the switching loss and inductor loss are almost same as the conventional one.

Unlike the traditional back-to-back converter which features a symmetrical structure, the loss distribution on the top, middle, and bottom switches in the proposed converter are not even. As shown in Fig. 11(b), due to the middle switch shared by two sets, in general the middle three switches dissipate more than twice the loss of those from the top three and bottom three switches.

From Fig. 11(c), it can be seen that the efficiency of both proposed and conventional converters follows a similar trend with the increase of output power. Also, the efficiency of the proposed converter is 0.5% higher than the traditional one. However, the efficiency still decreases with the increase of frequency due to the increase of the switching loss (see Fig. 11(d)).

The output power factor affects the sum of input and output currents, and ultimately influences the conduction loss. As shown in Fig. 12, the conduction losses are slightly increased as the output power factor is decreased.

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**Fig. 11. Comparison between conventional and proposed converter**
V. SIMULATION RESULTS

The simulation parameters are the same as those given in the efficiency calculation shown in TABLE II. The driving signals of three switches ($S_{al}, S_{ab}, S_{ad}$) are shown in Fig. 13(a). Fig. 13(b) shows the measured grid-side current and output line-to-line voltage with unity power factor operation. It should be noted that the control of the rectifier and inverter is decoupled, and therefore, the inverter operation will not affect the operation of the rectifier. The harmonic spectrum distribution is presented in Fig. 13(c).

Since the proposed topology inherits favorable 3-level converter characteristics, the THD of the output voltage is lower compared to the nine-switch converter shown in Fig. 14.

Fig. 15 shows the dynamic response of the proposed converter when the load steps between 15kW and 30kW. It can be seen that the load voltage is maintained smoothly and the voltage drop is quite small.

As previously analyzed, when two outputs of this converter are operated at different frequency, the modulation index sum of both sets will be restricted to unity. Fig. 16(a) shows the voltage waveforms when $m_{Top}=0.6$ (50Hz), $m_{Bottom}=0.4$ (60Hz) and $m_{Top}+m_{Bottom}=1$. If the $m_{Top}+m_{Bottom}>1$, the output voltage of the bottom set will be distorted as shown in Fig. 16(b).
VI. CONCLUSION

A component minimized dual output multi-level converter topology with reduced number of switches has been proposed. Three typical applications for the proposed converter were explained, and the dc-bus utilization was calculated. It has been shown that there is no reduction of the modulation index when both sets of output voltages have the same frequency and same phase. In the online UPS application, the efficiency was analyzed to demonstrate that the proposed converter achieves at least 0.5% higher efficiency compared to the traditional back-to-back 3-level converter while employing less number of switches. Finally, simulation results have been shown to demonstrate the validity of proposed topology.

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