Monolithic Reconfigurable SC Power Converter with Adaptive Gain Control and On-Chip Capacitor Sizing

Ling Su
Student Member
IDT
5670 N kolb, Tucson, AZ
lings@email.arizona.edu

Dongsheng Ma
Senior Member
The University of Arizona
1230 E Speedway, Tucson, AZ, 85721
ma@ece.arizona.edu

Abstract — This paper presents a monolithic reconfigurable step-down switched-capacitor (SC) power converter for self-powered microsystems. The design features an efficient step-down SC power stage with adaptive gain control and on-chip capacitor sizing. The adaptive gain control helps the converter maintain high efficiency continuously. Meanwhile, the size-adjustable pumping capacitors allow the output voltage to be regulated at different desired levels, even with a constant by 50% duty ratio. The monolithic implementation effectively suppresses the switching noises and glitches caused by parasitic components resulting from traditional bonding, packaging, and PCB wiring. The design has been sent for fabrication with a 180-nm CMOS process. Post-layout fully-transistor based simulations show that the converter is capable of precisely providing a variable power supply Vout from 0.9 to 1.65 V. It achieves a maximum efficiency of 89%, when Vout is regulated at 1.65 V and at a switching frequency of 4 MHz.

Index Terms— Reconfigurable, Adaptive gain control, on-chip capacitor sizing, switched-capacitor power converter.

I. INTRODUCTION

Self-powered sensing devices and implantable medical microsystems have been proliferating in recent years. Such a device usually operates at ultra-low power level with assistance of a specially designed power management system. To achieve long operation lifetime and low system profile, monolithic system integration is rising to become very attractive in this scenario.

However, there are certain new design challenges in such a power system due to its unique operation environment and design specifications. Firstly, due to the instability of self-harvesting energy sources, such a device is mandated to operate under a wide input/output voltage range. As a result, it is much more difficult to maintain high efficiency than traditional designs with fixed input and output voltages [1–4]. Secondly, while microelectronics technology can be further explored for system miniaturization, fully on-chip power management designs still face numerous technical difficulties. Thirdly, almost all the power conversion circuits for these applications are switching converters. Although these converters provide high efficiencies and flexible power conversions, they generate severe EMI noise and have bulky system profile, due to the employment of inductive components. Linear regulators are not preferred here because it is difficult to maintain high efficiency and stability over a large drop-out range. As potentially the best alternative to these applications, SC converters become very appealing.

However, similar to their switch mode counterparts, new architectures and control methods should be investigated in order to adapt to the new design challenges associated with variable output, large dynamic transient, and low noise.

In this paper, as a reference solution to the new design challenges, we propose a monolithic reconfigurable step-down SC power converter with adaptive gain control and on-chip capacitor sizing. The rest of the paper is organized as follows. In Section II, we address the details of system architecture and design strategy. Section III verifies our design ideas with transistor-based HSPICE simulations. Finally, we conclude this research in Section IV.

II. SYSTEM ARCHITECTURE & DESIGN STRATEGY

Ideally, if we assume there exists no power loss in the controller and power stage of a SC power converter, its efficiency can be computed as

$$\eta = \frac{V_{out}}{G \cdot V_{in}} \times 100\%$$

(1)

Here, V_in and V_out are the respective input and output voltages. G represents the conversion gain. Eqn. (1) reveals that if V_out is much lower than GV_in, the efficiency is very low, even in the ideal case. This proves that if V_in or/and V_out need to vary within certain voltage ranges, it could be difficult to preserve high efficiency with a fixed conversion gain. For example, for a SC power converter with V_in = 1.8 V and V_out = 1.2 V, if V_out drops to 0.8 V and the converter maintains the original topology for the conversion gain of 2/3, the highest possible efficiency would be 66.67%! We thus propose the adaptive gain control and on-chip capacitor sizing techniques to overcome this problem. The details are addressed as follows.

A. Adaptive Gain Control Scheme

The power stage of the proposed SC power converter is shown in Fig. 1(a), which operates with a pair of complementary phases — $\phi$ and $\bar{\phi}$. Instead of using large capacitors and switches for a single fixed conversion gain implementation, we employ 4 pumping capacitors C_1, C_2, C_3, and C_4 and 20 switches. This allows the converter to be reconfigured with 5 different conversion gains. For instance, as depicted in Fig. 1(b), with a fixed input V_in, if
V\textsubscript{out} needs to drop from V\textsubscript{1} to V\textsubscript{2}, the duty ratio should not be modulated since it would degrade the efficiency. Instead, the converter will be automatically reconfigured with a conversion gain change from G\textsubscript{3} to G\textsubscript{3}.

When the SC power converter reaches the steady state, the total net charge difference on the pumping capacitors C\textsubscript{1}, C\textsubscript{2}, C\textsubscript{3}, and C\textsubscript{4} should be equal to the charge consumed by the loading resistor R\textsubscript{L}, meaning that

\[
\left(C_1 + C_2 + C_3 + C_4\right) \left(V_{in} - V_{out} - \frac{1}{2}V_{out}\right) = \frac{V_{out}^2}{R} T
\]

Here, T is the switching cycle of the SC power converter. With C\textsubscript{1}=C\textsubscript{2}=C\textsubscript{3}=C\textsubscript{4}=C\textsubscript{p}, we obtain

\[
V_{out} = \frac{2V_{in}}{3T + RC_p}
\]

Hence, if \(\frac{3}{RC_p} \ll 3\), then

\[
V_{out} = \frac{2V_{in}}{3}
\]

Thus, a step-down voltage conversion of 2/3 is achieved.

For example, if V\textsubscript{out} is desired to be regulated at 0.6V\textsubscript{in}, the most appropriate conversion gain would be 2/3. As illustrated in Fig. 2(a), during \(\Phi\), the power switches S\textsubscript{1}, S\textsubscript{2}, S\textsubscript{3}, S\textsubscript{4}, S\textsubscript{10}, S\textsubscript{11}, S\textsubscript{12}, S\textsubscript{13}, and S\textsubscript{14} are turned on. This action charges up the pumping capacitors C\textsubscript{3} and C\textsubscript{4}. In the meanwhile, the charge accumulated in C\textsubscript{1} and C\textsubscript{2} is released to V\textsubscript{out}. During \(\overline{\Phi}\), the switches S\textsubscript{1} ~ S\textsubscript{6}, S\textsubscript{11}, S\textsubscript{12}, S\textsubscript{14}, S\textsubscript{17} are turned on, as shown Fig. 2(b). Accordingly, C\textsubscript{1} and C\textsubscript{2} are charged up while C\textsubscript{1} and C\textsubscript{2} discharge the power to V\textsubscript{out}. Note that if C\textsubscript{1}=C\textsubscript{2}=C\textsubscript{p}, the voltage across the capacitors C\textsubscript{1} and C\textsubscript{2} (C\textsubscript{3} and C\textsubscript{4}) will be equal to V\textsubscript{in}−V\textsubscript{out} (V\textsubscript{out}/2) at the end of \(\Phi\), and be equal to V\textsubscript{out}/2 (V\textsubscript{in}−V\textsubscript{out}) at the end of \(\overline{\Phi}\). When the SC power converter reaches the steady state, the total net charge difference on the pumping capacitors C\textsubscript{1}, C\textsubscript{2}, C\textsubscript{3}, and C\textsubscript{4} should be equal to the charge consumed by the loading resistor R\textsubscript{L}, meaning that

\[
\left(C_1 + C_2 + C_3 + C_4\right) \left(V_{in} - V_{out} - \frac{1}{2}V_{out}\right) = \frac{V_{out}^2}{R} T
\]

Also, the voltage across the capacitors C\textsubscript{1} and C\textsubscript{2} (C\textsubscript{3} and C\textsubscript{4}) will be equal to V\textsubscript{in}−V\textsubscript{out} (V\textsubscript{out}/2) at the end of \(\Phi\), and be equal to V\textsubscript{out}/2 (V\textsubscript{in}−V\textsubscript{out}) at the end of \(\overline{\Phi}\). When the SC power converter reaches the steady state, the total net charge difference on the pumping capacitors C\textsubscript{1}, C\textsubscript{2}, C\textsubscript{3}, and C\textsubscript{4} should be equal to the charge consumed by the loading resistor R\textsubscript{L}, meaning that

\[
\left(C_1 + C_2 + C_3 + C_4\right) \left(V_{in} - V_{out} - \frac{1}{2}V_{out}\right) = \frac{V_{out}^2}{R} T
\]

Here, T is the switching cycle of the SC power converter. With C\textsubscript{1}=C\textsubscript{2}=C\textsubscript{3}=C\textsubscript{4}=C\textsubscript{p}, we obtain

\[
V_{out} = \frac{2V_{in}}{3T + RC_p}
\]

Hence, if \(\frac{3}{RC_p} \ll 3\), then

\[
V_{out} = \frac{2V_{in}}{3}
\]

Thus, a step-down voltage conversion of 2/3 is achieved.

More specifically, Table I elaborates the switching schemes for the converter’s reconfiguration. Once the desired V\textsubscript{out} level is identified, the conversion gain is determined by the controller accordingly. The power switches will then follow the switching schemes in Table I to charge the pumping capacitor(s) and deliver the power to V\textsubscript{out}.

For example, if V\textsubscript{out} is desired to be regulated at 0.6V\textsubscript{in}, the most appropriate conversion gain would be 2/3. As illustrated in Fig. 2(a), during \(\Phi\), the power switches S\textsubscript{1}, S\textsubscript{2}, S\textsubscript{3}, S\textsubscript{4}, S\textsubscript{10}, S\textsubscript{11}, S\textsubscript{12}, S\textsubscript{13}, and S\textsubscript{14} are turned on. This action charges up the pumping capacitors C\textsubscript{3} and C\textsubscript{4}. In the meanwhile, the charge accumulated in C\textsubscript{1} and C\textsubscript{2} is released to V\textsubscript{out}. During \(\overline{\Phi}\), the switches S\textsubscript{1} ~ S\textsubscript{6}, S\textsubscript{11}, S\textsubscript{12}, S\textsubscript{14}, S\textsubscript{17} are turned on, as shown Fig. 2(b). Accordingly, C\textsubscript{1} and C\textsubscript{2} are charged up while C\textsubscript{1} and C\textsubscript{2} discharge the power to V\textsubscript{out}. Note that if C\textsubscript{1}=C\textsubscript{2}=C\textsubscript{p}, the voltage across the capacitors C\textsubscript{1} and C\textsubscript{2} (C\textsubscript{3} and C\textsubscript{4}) will be equal to V\textsubscript{in}−V\textsubscript{out} (V\textsubscript{out}/2) at the end of \(\Phi\), and be equal to V\textsubscript{out}/2 (V\textsubscript{in}−V\textsubscript{out}) at the end of \(\overline{\Phi}\). When the SC power converter reaches the steady state, the total net charge difference on the pumping capacitors C\textsubscript{1}, C\textsubscript{2}, C\textsubscript{3}, and C\textsubscript{4} should be equal to the charge consumed by the loading resistor R\textsubscript{L}, meaning that

\[
\left(C_1 + C_2 + C_3 + C_4\right) \left(V_{in} - V_{out} - \frac{1}{2}V_{out}\right) = \frac{V_{out}^2}{R} T
\]

Here, T is the switching cycle of the SC power converter. With C\textsubscript{1}=C\textsubscript{2}=C\textsubscript{3}=C\textsubscript{4}=C\textsubscript{p}, we obtain

\[
V_{out} = \frac{2V_{in}}{3T + RC_p}
\]

Hence, if \(\frac{3}{RC_p} \ll 3\), then

\[
V_{out} = \frac{2V_{in}}{3}
\]

Thus, a step-down voltage conversion of 2/3 is achieved.
A size-adjustable capacitor can be implemented with a series of small size unit capacitors and switches. Its final capacitance size is determined by status of switches and connections of unit capacitors. For example, if all the switches in Fig. 3(a) are turned on, an equivalent capacitance of $C_{1a}+C_{1b}+C_{1c}+C_{1d}$ is achieved.

According to Table 1 and Fig. 1(b), with 5 selected gain values, the biggest voltage gap ($\Delta V = V_i - V_{i-1}$, $i=2, 3, 4, 5$) between adjacent desired regulation voltages $V_i$ and $V_{i-1}$ is 200 mV if the converter is designed with a 1.8-V input voltage, 800-Ω load, and 50% duty ratio. 4 sizable on-chip capacitors are thus implemented here to control the regulation error to be below 50mV. As illustrated in Fig. 3(a), on-chip capacitor sizing “fine tunes” the regulation errors and thus helps to retain high efficiency.

Fig. 3(a) Size-adjustable switched capacitor, and (b) scheme of applying on-chip capacitor sizing to adaptive gain controlled SC power converter.

From the perspective of circuit implementation, with reference to Fig. 1(b), the regulator cells I, II, III and IV are each implemented with 4 sub-cells. For example in Fig. 4, Cell I actually consists of sub-cells I-a, I-b, I-c and I-d. These sub-cells employ a common topology but different sizes of switches and capacitors, tailored for different regulation voltage levels. Eventually, based on the common charge and discharge switching behaviors, they are grouped as A, B, C, D, as depicted in Fig. 5. Such a grouping method ensures the most efficient chip area and layout routing.

Fig. 4 Capacitor sizing in Cell I of Fig. 1(a).

C. Closed-Loop System Implementation

To illustrate the design idea, we consider the case when the conversion gain $G_2$ is 2/3 again. With reference to Fig. 3(b) and Eqn. (3), in order to allow the converter to regulate at the highest voltage in this region $V_{23}$, all the 16 sub-cells from I-a to IV-d function actively. As a result, the largest on-chip capacitor is generated as the sum of total unit capacitors. If $V_{out}$ needs to drop to the next voltage level $V_{22}$, all the sub-cells except those in the group D will stay active. Accordingly, the equivalent capacitance would be equal to the sum of total unit capacitance in the groups A, B and C. Similarly, if only one group A remains active with the topology of 2/3 gain, as shown in Fig. 3(b), the lowest output voltage in the region $V_{20}$ would be achieved.

Fig. 5 Block diagram of the proposed closed-loop design.

Fig. 5 illustrates the block diagram of the proposed closed-loop SC power converter. The output voltage $V_{out}$ is scaled and sampled, which is then compared to a reference voltage $V_{ref}$. Based on the error voltage between $V_{out}$ and $V_{ref}$, a frequency modulator determines the instantaneous switching frequency. For this design, the frequency varies from 4 to 8 MHz to suit different charge and discharge requirements. In the meanwhile, the proposed adaptive gain controller generates 3-bit gain control signals $k_3k_2k_1$, according to the instantaneous input voltage $V_{in}$ and the desired output voltage $V_{ref}$. The power stage is then reconfigured according to the proposed switching schemes in Table I. As a parallel process, the on-chip capacitor controller determines the active groups of sub-cells shown in Fig. 5, with a 2-bit control signal $l_2l_1$. 

2715
The control signals are then sent to a control signal generator to activate the desired switching actions in the power stage.

D. Design Extension to Variable-Input Constant-Output SC Power Converters

The proposed adaptive gain control and on-chip capacitor sizing techniques can also be applied to variable-input and constant-output converters. This is extremely attractive in the cases when an application has very unstable self-harvested input power source. The approach, similar to the one used in Section II-B, is illustrated in Fig. 6. The only difference under this operation scenario is that the highest (lowest) gain and largest (smallest) pumping capacitors size are applied to the lowest (highest) input voltage to obtain a constant output voltage. For example, the lowest input V53 operates with the help of all the sub-cells and the highest gain G5. A slightly higher input voltage V52, will still employs the same power stage topology and thus the conversion gain, but all the sub-cells in the group D would be shut down to reduce the total on-chip capacitance.

III. SIMULATION RESULTS

The proposed SC power converter is designed, simulated and fabricated with IBM 180-nm CMOS process. The layout is shown in Fig. 7. The on-chip capacitor implementation not only saves on-chip pads and IC pins, and largely reduces the system volume, but also minimizes the parasitic components caused by bonding, packaging, and PCB wiring; especially the ESR, ESL and ESC. These parasitic components are major contributors to large switching noises in power converter designs. For instance, if just the bonding parasitic effect is considered, each gold bonding wire contributes 0.257-Ω ESR, 5.869-nH ESL, and 0.242-pF ESC for 5-mm length [6].

All the power stages and buffers are optimized at a load with equivalent resistance of 800 Ω. The simulation efficiency is shown in Fig. 8. The output voltage varies from 0.9 to 1.65 V with a 1.8-V input voltage and a variable switching frequency from 4 MHz to 8 MHz. It achieves power efficiencies higher than 74% over the entire power range, with a maximum of 89% and the output Vout is regulated at 1.65 V. To summarize this work, Table II compares this design with the prior arts. The proposed reconfigurable SC power converter demonstrates a more area and power efficient solution.

<table>
<thead>
<tr>
<th>TABLE II. PERFORMANCE COMPARISON WITH PRIOR ARTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
</tr>
<tr>
<td>Process (CMOS)</td>
</tr>
<tr>
<td>Vin (V)</td>
</tr>
<tr>
<td>Vout (V)</td>
</tr>
<tr>
<td>Power (mW)</td>
</tr>
<tr>
<td>η</td>
</tr>
<tr>
<td>Chip area (mm²)</td>
</tr>
<tr>
<td>Pumping capacitance</td>
</tr>
</tbody>
</table>

IV. CONCLUSIONS

In this paper, we propose a new monolithic reconfigurable step-down SC power converter with adaptive gain control and on-chip capacitor sizing. The design features an efficient step-down SC power converter with multiple conversion gains and size-adjustable pumping capacitors, which are fully integrated on-chip to decrease the system volume and noise.
The number of I/O pins and on-chip bonding pads as well as parasitic components is significantly reduced. The design provides a high performance solution to monolithic power supply designs for new-generation self-powered devices.

ACKNOWLEDGEMENT

This project is sponsored by National Science Foundation under the contract of NSF CMMI 0925678.

REFERENCES


