FEASIBILITY OF MODERNIZING F-15 AVIONICS USING AN OPEN SYSTEMS APPROACH

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Background
The F-15 has been the world's premier Air Superiority fighter for many years, with an unequalled combat record. However, some of its avionics subsystems are now more than 20 years old and are experiencing both performance limitations and parts obsolescence problems. In this paper we describe an investigation into solving these problems by means of an Open Systems approach that maximizes the use of off-the-shelf technology. Our study focused on three of the avionics subsystems on the F-15 A-D model aircraft: the Central Computer, the Programmable Signal Data Processor, and the Head Up Display Signal Data Processor. We considered the feasibility of replacing all three subsystems with a single new unit, informally dubbed the Central Computer Display Processor (CCDP). Our method was to analyze the requirements of a notional CCDP, then investigate available technology for meeting those requirements. Where possible, we evaluated potential solutions by testing them in the F-15 Avionics Integration Support Facility (AISF). Our study culminated in a laboratory demonstration, which showed that a significant number of the F-15 central computer and display processing functions could be achieved using off-the-shelf technology. The Open Systems approach has great potential for extending the service life of F-15A-D model aircraft at a reasonable cost.

Requirements
Current Aircraft Configuration
The current F-15 avionics are shown in Figure 1. This study focused on the three Line Replaceable Units (LRU) highlighted in the figure.

VHSIC Central Computer
The VHSIC Central Computer (VCC) is the core processor of F-15 avionics. Data from various other F-15 avionics equipment are communicated to the VCC via multiplex electrical busses. The VCC processes this data and issues commands and data to the other avionics units. The VCC Operational Flight Program (OFP) implements functions required for the air superiority role, including Navigation, Controls and Displays, and Air to Air Combat. It is written in the Ada 83 programming language. The VCC hardware is a complicated multi-processing system that incorporates 7 processors, each executing the MIL-STD-1750A instruction set.

HUD Signal Data Processor
The Head Up Display (HUD) Signal Data Processor (SDP) generates stroke video signals to drive the HUD. There is no OFP for this device - its capabilities are "hard-wired". This has become an operational limitation in that air crews have requested HUD display changes that are impossible to accomplish with the current hardware.

Programmable Signal Data Processor
The Programmable Signal Data Processor (PSDP) generates the stroke symbology and raster video signals required to drive the Vertical Situation Display (VSD) and the Multi-Purpose Color Display (MPCD). In addition, the PSDP processes pilot selections via bezel switches mounted on the MPCD. The PSDP also processes a variety of other signals, including fuel quantity, stick position, roll rate, stabilator position, Fighter Data Link (FDL) discrete, radar serial data, and Data Transfer Module (DTM) serial data.
Figure 1: Current F-15 System Architecture

Figure 2: Proposed F-15 System Architecture
Limitations of Current Avionics

Obsolescence
The Air Force faces parts obsolescence problems with each of the three avionics units we investigated and these problems are expected to be critical within the next five years.

Operational Limitations
There are several known limitations with these avionics units. For example, the newer F-15E model aircraft have a HUD pitch ladder which is "graduated", which means that the symbology changes as pitch increases, providing the pilot with a clearer visual indication of his attitude. This is a significant improvement from a flight safety perspective. Unfortunately, it cannot be implemented using the current HUD SDP. A similar situation exists with regard to displaying missile type identification on the HUD. From an operational point of view, improvements in these areas are highly desirable, but impossible with the existing hardware.

Software Cost Driver
The VCC and PSDP currently have significant resource constraints in terms of throughput, memory, and bus bandwidth. These constraints tend to drive the cost of software development higher, since even a small change may require considerable design and testing effort if existing capability must be removed or rewritten to free up resources for the new capability.

Proposed Aircraft Configuration
The notional CCDP is required to be a Form-Fit-Function replacement for the VCC, with the additional functions of the HUD SDP and PSDP included. As such it must fit in the VCC mount and mate to the existing aircraft connectors. No aircraft modifications can be performed to install the CCDP; however, as a part of the modification kit, an adapter cable harness is an acceptable solution. Figure 2 shows the proposed aircraft configuration with the CCDP.

Open System Approach

System Architecture
In analyzing the system requirements, it was clear to us that they could be grouped into three broad categories: general purpose processing, communications, and display processing. In addition, we also looked at development tools for implementing the software.

An early architectural consideration was the choice of a backplane bus, by which the circuit cards within the new unit would communicate. Older avionics units, such as the PSDP and HUD SDP, typically utilize a proprietary backplane bus. The VCC uses a standard (although not widely adopted) bus, the Parallel Intermodule (PI) bus.

Candidate busses we considered were PI bus, VME bus, Compact PCI (cPCI), and VME-64. We selected VME-64 based on general commercial support and the wide variety of components available for it.

Similarly, the VCC and PSDP OFPs incorporate their own custom executive. We chose VxWORKS, a commercial Real Time Operating System (RTOS) that is widely used for embedded computer applications, as the underlying operating system for the CCDP.

General Purpose Processing
Hardware
For general purpose processing, there are a number of high performance processors available for VME-64-based systems. We chose what is perhaps the most commonly used within newer military systems, the Motorola PowerPC family. Ruggedized PowerPC boards that meet military environmental specifications are available from several sources. For our technology demonstration, Lockheed Martin Systems Integration (LMSI) of Owego, New York, provided us with an SP-103A PowerPC board, which is their second generation PowerPC product.

1 VxWorks is a trademark of Wind River Systems, Inc.
Software

Although the VCC OFP is mostly written in the Ada 83 programming language, some functions are implemented in MIL-STD-1750A assembly language. Ada language programs are highly transportable across target platforms, but assembly language programs are generally not transportable at all. We had two choices for the software baseline that would be used: the fielded Operational Flight Program, which would require rehosting of the Ada source and rewriting of the assembly language portion; or the Rapid Prototyping System (RPS) baseline, which was already targeted to execute on a PowerPC. Rewriting a significant amount of assembly code to run on a PowerPC was outside the scope of this study; therefore, the team chose the RPS baseline as a starting point. Even though the RPS software was targeted to execute on a PowerPC, numerous changes to the code were required in order to make the program run properly.

Communications

Communications external to the CCDP can be categorized as MIL-STD-1553B, H009, and miscellaneous other interfaces.

MIL-STD-1553B Bus

Two dual redundant MIL-STD-1553B channels are included on-board the LMSI SP-103A processor board, so the F-15C/D interface hardware requirement was easily met. From a software perspective, a driver was required that would allow the VCC software to utilize this interface. The study team developed this driver software.

H009 Bus

While the H009 bus is a documented standard, it is used only on the F-15 aircraft. Consequently, there are relatively few vendors of H009 interface hardware. However, we were able to work with the H009 products of two different vendors, Excalibur Systems and Raytheon. As with the 1553 interface, there was a need to develop two different driver programs that would enable the VCC software to access these boards. The study team developed the driver software with support from the respective vendors.

Miscellaneous Interfaces

There are a wide variety of other interfaces required by the CCDP. They can be divided into two categories. First, there are some relatively common interfaces (i.e., analog, discrete, serial data) that can be met by readily available COTS boards. The implementation of these interfaces was deemed to be straightforward and no further effort was expended on them for the feasibility study. In the other category, however, are interfaces that are clearly unique to the F-15 application and require a custom designed and built solution. Given the limited scope of our effort, we did not attempt to develop and demonstrate hardware for these interfaces; however, discussions were held with a leading avionics vendor in order to quantify the risk and cost of developing hardware to implement these interfaces. There appears to be no significant technical risk and the cost can be reasonably estimated.

Display Processing

Hardware

In the F-15C/D both raster and stroke video display processing are required. Raster video is widely used commercially and is standardized; therefore raster video generation hardware is available from several sources. We were able to use an LMSI mezzanine graphics board to generate raster video. The LMSI graphics board utilizes OpenGL® API (Application Programming Interface) and produces RS-170 RGB raster video. We decided to implement representations of the HUD and MPCD symbology on standard monitors using the available raster video, thus demonstrating some display processing capability of both the HUD SDP and the PSDP.

Stroke video is much less commonly used and is not standardized. The result is that stroke video generation hardware must be a custom design. Given the limited scope of our effort, the we did not attempt to develop and demonstrate stroke video generation hardware; however, discussions were held with a leading avionics vendor in order to quantify the risk and cost of developing such hardware. There appears to be no significant

*OpenGL is a registered trademark of Silicon Graphics Inc
technical risk and the development and production costs can be reasonably estimated.

**Software**

The existing PSDP software is written in a unique assembly language, while the HUD processing is implemented in hardware. Therefore, new software was developed to implement the display processing functions required for the feasibility study. The purpose was to determine the effort and risk associated with developing an entire display processing function for the F-15A-D. In keeping with the Open System approach, we chose to use the OpenGL API running on X windows to develop this display software. Both OpenGL and X windows are standardized and well supported commercially. We used the Seaweed Systems Inc implementation of these items.

The symbols used by the HUD SDP were implemented in a C program using OpenGL calls to generate the graphic representations. All of the HUD symbols were converted and tested statically; most were tested dynamically.

The VCC drives the PSDP with “macro” instructions that describe the graphical displays the PSDP is to generate. The PSDP OFP macro compiler was rewritten in C using OpenGL calls to generate representative MPCD displays. Only the most frequently used macro instructions were implemented for the purposes of this study, which allowed for seven of the fourteen MPCD display formats to be generated.

**Software Development Tools**

In recent years the “Open Source” movement, largely initiated by Richard Stallman of the Free Software Foundation, has resulted in readily available, no-cost, high-quality software development tools. To evaluate the feasibility of using these tools for avionics applications, the study team adopted several of them for this effort. Specifically, we built from open source the gnu C and GNAT Ada compilers, hosted on a PC running Linux and targeted to the SBC-103A PowerPC running VxWorks. In general we were impressed with the quality of these toolsets.

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**Figure 3: Software Architecture CCDP**

Reused ~80% Existing Code

- Rehosted VCC OFP (Ada)
- New Display Processor OFP (C)

New Development

- COTS Software Product
- PCI Bus to Graphics Processors

Hardware

- VxWorks
- I/O Drivers
- OpenGL

1553

VME

Ethernet to Backup Processor

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Technology Demonstration

The demonstration included testing in the F-15 Avionics Integration Support Facility (AISF), located at Robins Air Force Base. The AISF is a software integration facility used to develop and test OFP block cycle changes for F-15 aircraft. The AISF consists of several integration benches that provide real-time, closed-loop, hardware-in-the-loop, integration of F-15 avionics hardware and software, with full non-intrusive diagnostic monitoring capability.

On 27 September 2000, the study team presented a technology demonstration to the F-15 senior engineering management. The demonstration consisted of a VME-based system inserted in the Cockpit Integration Bench (CIB) in the F-15 AISF. The demonstration system contained one SP-103A processor, one graphics mezzanine processor, and two H009 interface cards (one from Excalibur and one from Raytheon). The VME-based processor replaced the VCC, PSDP and HUD SDP in the AISF CIB. A dynamic scenario involving changing displays, flight regimes and system functions was conducted. We demonstrated general purpose processing, communications on both MIL-STD-1553B and H009 busses, and generation of both HUD and MPCD displays. This exercise showed the technical feasibility of modernizing F-15A-D avionics via an Open Systems approach.

Conclusions

In this paper we have described our investigation into applying an Open Systems approach to upgrading the avionics subsystems on the F-15 A-D aircraft, looking specifically at the Central Computer, the Programmable Signal Data Processor, and the Head Up Display Signal Data Processor. Where possible, we evaluated potential solutions by testing them in the F-15 Avionics Integration Support Facility (AISF). Our study culminated in a laboratory demonstration, which showed that a significant number of the F-15 central computer and display processing functions could be achieved using off-the-shelf technology. The Open Systems approach has great potential for extending the service life of F-15A-D model aircraft at a reasonable cost.

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Figure 4: Technology Demonstration Hardware