DESIGN OF A POWER-OPTIMIZED MICRO MINIATURE ADVANCED INSTRUMENT CONTROLLER FOR SENSOR CRAFT APPLICATIONS

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ABSTRACT

A highly-functional self-contained sensor data acquisition and processing system is under development for a probe designed to penetrate the surface of Mars. The processing system, based on an 8051 controller, is about the size of a postage stamp, weighs three grams, and consumes 50mW in nominal operation. It is designed to operate in space under 15,000G impacts and down to -120°C temperatures. Though small, its 32 analog inputs, six serial ports, 32 digital interface lines, eight analog outputs, and in-situ reprogrammability make this device attractive for direct application in many aerospace systems.

INTRODUCTION

Space computers are among the most costly and sophisticated electronics subsystems in modern spacecraft. Not surprisingly, extensive research has been poured into making space computers of steadily increasing sophistication, with one or more 32-bit central processing units (CPUs), large memory stores, complex backplanes, and arrays of protocol-intensive wire and optically based interfaces. Oddly, however, it seems that the need for simple, commodity-oriented controllers could not have altogether vanished, though this gap has not been addressed in present research efforts.

As a possible solution, this paper describes the design of a novel space-qualified “midget” computer microcontroller, design expressly to meet modest spacecraft data handling and processing needs through a relatively rich, system-oriented set of built-in resources. The genesis of the concept stemmed from a need for an extremely low-overhead computer for a space experiment. At the same time, it was recognized that a minimalistic computer could serve ideally in many applications, ranging from peripheral, sub-tier processors in large satellites to the central computer of very simple spacecraft. It was in the pursuit of the latter that led to a program to develop the Advanced instrument Controller (AIC) for application in the NASA New Millennium Program’s Deep Space II (DS2) mission. As will be shown, the requirements of even a modest controller that must operate as the “brains” of a projectile propelled into the surface of a planet are non-trivial. Nevertheless, a surprisingly capable, if not spartan self-contained computer has been formulated to meet the needs of this mission.

The major features and components of the AIC design will be described, along with the unique solution adopted for packaging, test, and assembly.

The Deep Space 2 Sensor-Craft Controller

AIC responds to extraordinary design demands for a low-power micro-miniature data handling system to be used in the NASA New Millennium Program. The current design promises to shatter previous performance, power, and cost points for space-qualified stand-alone computers. The design is based around a very small (25mm x 30mm) patterned overlay multichip module (MCM), which contains a customized radiation-tolerant 8051 8-bit microcontroller, 128 kilobytes of static RAM, 128 kilobytes of non-volatile storage, on-board startup and clock circuitry, and a compact arrangement of large amounts of built in peripheral support. Total module power consumption is designed to be less than 50mW at five megahertz. The module itself is designed to function after 15,000-G shock loads and will operate at temperatures as low as -120 °C. Part of the power reduction strategy involves optimizing the design of two integrated circuits for the reduced capacitance represented by millimeter scale interconnections within the interior of the MCM. The approach chosen will result in a packageless, few-chip MCM with
relatively low cost potential as compared to the more cumbersome conventional and MCM configurations typically found in contemporary space-grade computers. Due to the synergistic combination of these attractive features, the module is expected to have widespread appeal, and independent internal research is underway to explore the use of this design for a generic cryocooler control replacement. The design paradigm for this module is based on the concept of combining modest quantities of processing and memory with generous amounts of analog and digital interface capability in a self-sustaining design, inspired by highly integrated designs in the commercial marketplace, such as the very successful Microchip (Chandler, AZ) PIC microcontroller series.

MISSION REQUIREMENTS

A brief review of the Deep Space II (DS-2) mission serves to justify various aspects of the design of the Advanced Instrument Controller (AIC) [1]. The AIC is designed to be contained within each of two microprobes that are to be dropped into the Martian atmosphere via aeroshells. Figure 1 illustrates the location of the two aeroshells on the Mars 98 Surveyor, which will serve as the host vehicle. As shown in a cross section of an aeroshell (Figure 2), the probe accounts for only a relatively small portion of volume. The aeroshell provides the necessary aerodynamic stability for the ballistically guided penetrator probes to impact the Martian surface in the correct orientation. The probe design itself is based on a highly novel two-piece construction. Figure 3 depicts the relative configuration of the two sections during the impact sequence onto the Martian surface. Of the two sections, the "pancake section" undergoes the highest impact forces (as high as 80,000G’s), while the penetrator section experiences some deceleration from the soil (up to 15,000G’s). A flexible cable provides power and signal interconnection between the two sections. Equilibrium temperature for the penetrator will likely be a narrow excursion about a final temperature somewhere between -80°C to -120°C. Many uncertainties exist with the mission. For example, it has been estimated that a 3% chance exists for the probes to impact a rock upon impact, which would destroy the probes.

Mission Profile

Except for the last 240 seconds of the flight from Earth to Mars, the microprobes remain unpowered. It is suggested that this short time window is the only point in the mission where radiation effects, particularly single event effects, pose any sort of problem. The mission profile from “power on” through impact and subsequent data gathering activities are captured in the Figure 4 mission timeline. During deceleration, data is gathered to understand the transitions to atmosphere and to the initial surface impact. Shortly after impact, the most significant set of experiments, including a sophisticated instrument to examine moisture content in a minute soil sample, are executed. For the remainder of the short mission (about 14 days), data on temperature and pressure are periodically gathered and uploaded to an orbiting host, which orbits Mars. Periodically, state information is written to an on-board non-volatile memory. This state preservation capability is needed, as it has been determined that the surface temperature on Mars may fall below the point at which the primary batteries can function, mostly due to shading effects. As the surface temperature rises again, the DS2
probe would revive, restoring its operational context based on the state information in non-volatile memory.

![Diagram of probe](image)

**Figure 3.** Two-section probe. (a) Transit. (b) Initial impact. (c) Separation.

**DESIGN OF THE ADVANCED INSTRUMENT CONTROLLER**

Many obvious constraints are imposed in designing a system controller for the DS-2 interplanetary microprobe. Despite the severe mechanical requirements, energy availability for the DS2 mission is such a difficult constraint that power management became a singularly dominant driver. The overall design chosen for the AIC, shown in Figure 5, is based on the desire to provide high utility at modest performance levels with minimum size, weight, and power. In this respect, the AIC was not intended to compete with high-performance microcomputers, but to augment them with simple instrumentation support and expanded communication circuitry. By achieving this in a small profile, it is possible to use many AICs in larger systems to dramatically simplify complex control, particularly related to health and status monitoring.

**AIC Features and Major Components**

The AIC provides the user with 128K bytes each of static and electrically erasable RAM, the latter being non-volatile and in-system reprogrammable if desired (reprogrammability is disabled by hardwire connection). Based on a 12-bit analog-to-digital convertor (ADC), the AIC can gather data from up to 32 channels at an aggregate rate of approximately 25 kHz. Eight digital-to-analog convertors (DACs) are also provided at 10-bit resolution for simple actuator or control requirements. A total of 32 digital channels are provided for logic level interfacing and switching, and six serial ports are provided to promote networking, simplify interfaces, and eliminate the need to expand circuitry in most applications. All these functions are provided at a nominal 50 milliwatt power budget within a 25 x 40 x 2 mm, 3 gram multichip module (MCM), which is reduced to below 100 microwatts in a retention / standby mode. Following is a more detailed description of key AIC components.

**CPU** - The central processing unit is a 3.3V unit, binary compatible with the 8-bit Intel 8031 / 8051 microcontroller, but with enhanced features and peripheral capability. A special provision was made to power-down the

![Block diagram of the Advanced Instrument Controller (AIC)](image)

**Figure 5.** Block diagram of the Advanced Instrument Controller (AIC).
EEPROM after boot-up to conserve power, which requires a second, completely isolated address and data bus, which isolates the first bus from dead driver loading. The additional analog and digital functionality is implemented in special function registers and memory mapping. To further enhance the performance of the 8051, portions of the AIC8051 are expanded to 12-bit data widths, improving throughput for higher data sampling rates. The need to support dual voltage levels —5V and 3.3V— placed further complexity onto the design of the AIC8051. Another important feature of the CPU is the provision for non-volatile data write-back to the EEPROM, implemented as a normally unused 8051 op code. Boeing (Seattle, WA) is performing the design of the enhanced 8051 CPU using a very sophisticated electronic design capability that allows rapid porting of the gate-level netlist to foundry processes. This capability provides a large set of implementation options, including fully radiation hardened fabrication lines.

Analog - An analog support integrated circuit (design by Technology Associates Group, CA) operating on a 5V supply provides a customized low-power extension for analog input and output from the AIC. A total of up to 32 analog input voltages with 0-4.096V span can be directly interfaced to the AIC at 12-bit resolution. Up to eight analog outputs are available at 10-bit resolution. Through the use of very conservative design rules and off-chip precision resistor arrays, the no-trim design of the analog support chip for the AIC assures maximum flexibility for fabrication through a number of industry sources.

Memory components- Selections for memory devices for the AIC are limited to existing devices. As such, finding components with the unique combination of requirements (known radiation performance, functional to -120 °C, 3.3V operability) is a significant challenge. Current investigations have led to the selection of Hitachi SRAM and EEPROM components, which are the closest to meeting the unusual set of requirements for the DS2 mission.

Other components and features- The AIC can self-start from its own 10MHz internal clock or through an externally supplied low-frequency clock (e.g., 32 kHz), which allows the AIC to take advantage of at least two other precision clock sources in the DS2 probe.

PACKAGING AND TEST APPROACH

The AIC construction approach employs a tightly-coupled MCM design based on a new extension of the high density interconnect (HDI) process. The standard HDI process (Figure 6) embeds integrated circuits (ICs) and other components into a substrate (Figure 6a-6b), usually made of ceramic. Through the use of a patterned overlay (Figure 6c-6d), the contact terminals of all components are simultaneously interconnected, resulting in a compact, high-performance MCM. In the AIC module, a new version of HDI which employs plastic substrates will be explored. The introduction of a plastic as a substrate material will reduce cost (no substrate milling required) and weight, while improving mechanical robustness.

The floor plan of the AIC is shown in Figure 7. In this figure, “AD” refers to the analog IC, “EE” refers to the EEPROM, “C” refers to a decoupling capacitor, and “R” refers to customized resistor arrays used by the analog IC. The AIC design employs “tightly-coupled” MCM design techniques, which basically refers to exploiting lower capacitance in the MCM interconnections to reduce overall consumption. Since power consumption can be expressed as:

\[ P = C \cdot V^2 f \]

(where C is capacitance, V is voltage, and f is frequency), reduction of

Figure 6. High Density Interconnect (HDI) standard process. (a) Milling. (b) Die placement. (c) Overlay lamination. (d) Interconnection formation.
capacitance and voltage for a given frequency are necessary for power reduction. Since native MCM interconnections for a small substrate design manifest significantly reduced capacitance over a design built as an ensemble of single chip packages (by about one order of magnitude), a significant opportunity for power reduction exists, especially if voltage is simultaneously reduced. Two simple measures carried out in the IC design exploit the MCM’s lower capacitance directly: (1) reduced geometry for native IC driver, and (2) physically smaller bond pads. While closely coupled MCM methodologies result in more efficient designs, at least two additional problems are presented. First, optimized pad driver design techniques cannot be readily applied to any signal conductors that must “escape” outside the MCM, since capacitance is increased. Second, the diagnostics of tightly-coupled MCMs and their components is not an established practice. Their existence poses a far greater challenge to the so-called “known-good-die” problem than do today’s typical integrated circuits. The testing strategy for the AIC is partly provided by the packaging technology itself. Since the patterned overlay MCM arranges components onto a planar substrate, why not exploit the substrate as a test fixture? By asserting a design procedure for the first metal layer of the MCM to perform the function of re-distributing the electrical contacts of all ICs in a uniform grid for test access, alignment criticality is reduced considerably when compared to aligning directly onto the IC bond pads (Figure 9). Also, common power and ground nodes are combined in this redistribution approach, reducing the problem of efficient power delivery. Hence, the partially fabricated MCM is amenable for direct physical test probe access by using a specially-fashioned socket, not unlike a socket for a ball grid array package (Figure 10). Though the reduced drive capability of the closely-coupled IC design does not permit full-speed test due to capacitive loading of the test fixture, it is still possible to exercise the module at a reduced clock speed over a very wide temperature range (-120 °C to +80 °C).

Within the DS-2 microprobe design (Figure 8), all electronics are mounted onto small “T” beam structures, which are arranged as a triangular configuration (Figure 8b). Several possible mounting arrangements for an MCM are possible, but perhaps none as compact, simple, and direct as an integral ball grid array (BGA) package mounting approach. The HDI/BGA technique is diagrammed in Figure 11 as a simple post-processing sequence whereby conductor pads are formed on the top-level metal in the overlay of a fabricated HDI module and subsequent processing attaches solder spheres of controlled volume about the surface in a deliberate pattern to form a compliant contact system that facilitates the next level of assembly. The assembly procedure itself involves the reflow solder attachment of the BGA and the application of an underfilling compound for additional mechanical robustness.
CONCLUSIONS

This paper described the design of an advanced instrument controller (AIC) for low-power space operation in high-G and cold temperature environments. Though the unit functions as a self-supporting data acquisition unit, it is physically very small and low-powered. The arrangement of custom and off-the-shelf components within the framework of a tightly coupled MCM design is a key to achieving the levels of performance required in this design.

Although the AIC is designed to handle to special, rugged environments associated with its impact into the surface of Mars, it answers the need for a highly functional commodity data acquisition and processing system of modest proportions. As such, the AIC can perform simple sensing and control functions in distributed locations more efficient than general space-qualified computers. Many of the AIC features are optimized around reduced size, weight, and power, including the ability to preserve state information in the event of power removal.

ACKNOWLEDGEMENTS

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[1] The information in this section is derived from mission documentation, meeting notes, and handouts.