ABSTRACT
Recent tests have established upset levels for a set of digital flight control computers exposed to microwave radiation. Upsets occur for unprotected computers above 10 W/cm² peak power over narrow frequency bands. The frequency range of upsets were from 1 to 4 GHz, no upsets were seen above these frequencies due to increased attenuation from circuit elements. Most vulnerable frequencies are at box resonance, which lie in the low single GHz for these types of avionics. Upset levels can be an order of magnitude lower at box resonance. The main point of entry of the microwave radiation is the VO wire bundles. Box dimensions, wire runs, and internal board layout affect vulnerability. Almost all upsets seen were digital upsets. This is due to the very wide bandwidth of digital circuits being able to respond to narrow microwave pulses. The most important signal parameters to determine digital flight control computer upset potential are carrier frequency and peak power. Simple shielding techniques have the potential to eliminate any possible upsets seen.

INTRODUCTION
Over the last few years growing concerns about the possible upset of digital, fly-by-wire flight control systems (DFCS) by electromagnetic interference (EMI) have led to stricter design and testing requirements. Concerns exist that postulated high power microwave weapons, as well as powerful commercial broadcasting stations, will disrupt the normal operation of DFCS. Since the DFCS is a safety-of-flight system, normal operation in any adverse environment the system might be exposed to must be insured.

As part of a multi-service investigation into DFCS upset, the Air Force Wright Laboratory is characterizing the types of upsets that can happen within a DFCS when operating in an intense EMI environment. The goal is determining whether modifications to system architecture and algorithms, in addition to filtering and shielding, will mitigate any EMI problems found. This work was done under several programs over the last few years.

This paper reports on results of tests to one DFCS component, the digital flight control computer (DFCC). When integrated with other DFCS component test results, an overall idea of DFCS vulnerability to microwave radiation can be determined. The data in this paper is valid for microwave region, in the frequency range from 1 - 8 GHz. There is good reason to extrapolate our data to predict upset chances above 8 GHz, but lower frequencies cannot be extrapolated due to complex wiring, circuit, and other system effects. Some of these effects are covered in References 1 and 2.

DISCUSSION
Overview Of DFCC
A modern DFCS is actually a mix of analog and digital signals and technologies. Figure 1 is a simplistic block diagram of a generic digital flight control system. Aircraft motions are detected by gyros and accelerometers. These sensor signals, along with other sensors, such as control surface positions, stick position or force, angle of attack, and air data, are transmitted from the sensor to the DFCC on an analog bus. Once inside the DFCC, the signals are put through a series of analog filters (anti-aliasing, structural mode elimination) then digitized. The first gate the digitized information must pass is a 'sensor value worth' test. Redundancy management algorithms compare 'local' data with the data coming across the cross channel data link from the other computers. This software insures each sensor is working, that the sensor information is in a valid range, and picks (or calculates) a value for the computer to use in the control laws.
Flight control systems are AM modulated systems, they rely on amplitude signals sent by their sensors to properly control the aircraft flight path. The bandwidth of the stability augmentation loops are at most 3 Hz (from 0 to 3 Hz). This is due to two reasons, first of all very little pertinent information lies above since the aircraft (and pilot) can not respond quicker due to inertias, and second, higher bandwidths excite aircraft structural modes.

In order to meet safety of flight requirements, the computer channels are redundant, either triplex or quadruplex, and share extensive data to a) detect failures, and b) reduce transients if a failure occurs. Sensor redundancy depends on the flight criticality of the sensor. The motion detectors used to stabilize the aircraft, the gyro, accelerometers, and angle of attack probes, must meet system safety requirements. The computers are usually located in avionics bays near the front of the aircraft.

DFCS EMI protection is set forth in the procurement specification. Current testing levels for USAF flight critical systems is 200 V/m average free field from 10 kHz to 18 GHz. The same level of protection has been suggested for the commercial systems. Typical protection methods include filter pin connectors, shielded twisted pair balanced input/output lines, backshell connectors, and well constructed containers. No flight software algorithms check exclusively for EMI upset, but redundancy management algorithms will detect large enough deviations of DFCS signals due to EMI.

Description Of Test Articles

The DFCS tested composed of four equipment boxes, three identical DFCC and a box containing back-up servo actuator amplifiers. The computers operated asynchronously, and contained six circuit boards connected to a wire-wrap backplane. Five connectors on one box side attached the computers to the "outside world", four are connected during normal operation. The 625 wires on these connectors come straight into the backplane. The computer boards each contain about 100 small scale, medium scale, and large scale integrated circuits. The boards themselves are 15 layer multiwire boards with several internal ground planes. The box sides are made from milled aluminum welded together. Front and back panels are held on by multiple screws and have EMI and humidity gaskets. The box sides contain heat exchangers for cooling air. The only holes to the outside world are those which contain the cable connectors. Most input wires are analog, the only sharing of digital information being on several MIL-STD-1553B busses which allow the computers to talk to each other and other avionics. The computer internal architecture and electronics are typical of the type in digital systems flying today.

The computers each had several thousand hours of operation before our tests began. The front and back panels were removed numerous times before, and during, our tests. We feel that this represented the type of maintenance that the typical DFCC would see during it's lifetime, reflecting the influence on maintenance actions on EMI hardness.

The wiring used during the test program was the same type as is used in aircraft, the only difference was the longer length. The length was not a factor since only the first few wavelengths of wire at microwave frequencies act as the antenna due to attenuation.

The DFCC was equipped with an extensive variety of internal self-checking algorithms. Monitors covered data validity and constantly checked internal analog and digital circuit health as well as some external (to the DFCC) DFCS hardware. Any anomalies found were stored and reported to the other DFCCs and the DFCS monitoring computer in the test bench. In this way, the failure codes could be read out real-time while the testing was in progress.

Brief Rundown Of Tests

Three levels of test were performed on these computers during the January 1991 - April 1992 period.

1. Low Power Coupling Tests (LPC) - The unpowered boxes were instrumented with probes and exposed to low level microwave fields to determine the amount of microwave radiation leaking into a box, the points of entry of that radiation, and the effective antenna apertures of critical DFCS circuits. Six different box orientations and two polarizations were tested [3].

2. Direct Injection Tests (DI) - Microwave signals were injected directly into critical circuits while the boxes were operating. This determined the upset level of the circuits as a function of source frequency [4].

3. High Power Tests (HP) - The entire DFCC suite was set up, operational, in an anechoic chamber and exposed to free field radiation from several magnetron sources at field levels ranging from 0.5 W/cm² to above 400 W/cm² [5].
The tests built on themselves. From LPC we knew how much and where the energy gets in. From DI we knew the upset levels. From these we predicted the best signals to cause upset going into the HP tests and focused on those.

In the LPC and DI cases, source frequencies ranged from 0.5 GHz to 8 GHz. The free field tests were limited to two frequencies by the sources and chamber time available. CW sources were used for DI and LPC tests, pulse sources for HP. Responses from the different signal sources can be linked through Fourier analysis of the signals and circuits.

An upset was defined as any time the redundancy management software detected an anomaly and logged into computer memory, or the computer stopped functioning. The upset levels for analog signals depended on the signal affected. These were usually in the 0.1 - 1.0 V range in difference from nominal. Digital upset was caused by about a 1 - 2 V change in signal level.

Test Results

LPC

The LPC test showed that the major point of entry for microwave radiation into the DFCC was the cable bundle I/O wires coming through ports in the front panel[5]. The frequency of maximum coupling corresponded to a box resonance. Figure 2 is a comparison of the power measured at an input to the analog interface board with cables connected versus cables disconnected and ports sealed. The I/O bundles are dominant up to 4 GHz after which the internal energy is essentially equivalent to the "noise floor" measured with ports sealed. The data shows that internal test points do not receive much energy from the free field for frequencies above 5 GHz, seeing attenuations greater than 30 dB from 1 GHz values. This is normal for the type of wiring and circuit design used in the DFCC. The 26 gauge input and backplane wiring, circuit boards, and integrated circuits cannot pass, or respond to, the higher microwave frequencies.

The sealed box trace shows significant resonant peaks at several frequencies. The highest peak is at 1.3 GHz. This corresponds to the TE_{10} mode of the vertical box dimension. As opportunity would have it, these DFCC boxes have a depth twice the height. The box by itself is a resonant chamber. The coupling at this frequency is over 15 dB stronger due to the resonance.

Noise floor measurements taken inside the DFCC checked for leakage from instrumentation. These were also be used to check box shielding effectiveness. On the average, the box provided 15 dB attenuation in free field power levels over the 0.5 GHz to 8 GHz range tested.

Table 1 contains the average and greatest effective areas found for analog and digital circuits. It also contains the same area information for circuits connected directly to the I/O wire bundles and buried circuits on the boards.

These are general observations from the LPC data:

- Maximum coupling occurred at box resonant frequencies with radiation entering through cable ports.
- On the average, circuits with connections to the I/O wire bundles have 10 times the effective area as buried circuits.
- On the average, digital circuits have six times less effective area than analog circuits.
- If the circuit is digital and buried, the effective antenna area is small.

This data indicates that analog circuits connected to the input ports will experience the highest microwave radiation levels, buried digital the lowest. Whether or not they lead to upset depends on the upset level of the components. This was determined during DI tests.

DI

Figure 3 shows one of the principal results of the DI test, average upset power levels versus frequency for the types of circuit injected. This graph represents 187 separate upsets recorded during this test phase. The salient points learned during this test were:
- 1.3 GHz was the most sensitive frequency, driven by box resonance.

- The next minimum in the 1-10 GHz range is between 2.5 and 3 GHz.

- For the CW signals used, digital circuits required more power to upset than analog circuits.

- Above 4.3 GHz no upsets were recorded due to lack of source power. The hardness is due to increased circuit attenuation, and decreased rectification efficiency.

Analysis of the upset types and computer construction showed the majority of upsets seen were due to cross coupling on the backplane wiring. Many of the "digital upsets" seen were actually upsets of analog portions due to cross coupling on the backplane. Almost all of the analog upsets were due to cross coupling - the upsets occurred at other circuits than the ones being injected. The maximum sensitivity was at 1.3 GHz.

The upset levels for analog circuits between 1 and 8 GHz were always at a minimum at 1.3 GHz. Most of the digital circuits had their minimums at 1.3 GHz. The ones which did not had minimums at 3 or 4 GHz.

DFCC box construction was the major influence in LPC and DI tests effects. The vertical height being twice the depth lead to a strong box resonance at 1.3 GHz seen in the LPC test. The strong cross-coupling seen at 1.3 GHz in DI testing was due to the backplane wiring. The wiring is the same height as the vertical box dimension, thus also resonates at 1.3 GHz. The backplane wires are arranged vertically, leading to efficient pick up the TE mode energy and coupling it into a sensitive circuit. The boards are also arranged vertically, so the TE_{10} mode in the vertical plane (1.3 GHz) can propagate within the box (these same boards have ground planes within to negate modes in other directions). The synergism in backplane wiring, board mounting, and box design make 1.3 GHz the best frequency for microwaves to effect DFCC operation.

If the box internal configuration wasn't bad enough, the coupling was compounded by the designer's practice of bringing all grounds through the input connectors and grounding them to common grounds inside the box. This generated numerous loop antennas for the energy to couple from once inside the box.

Even with this built-in coupling configuration, the predicted upset field levels at 1.3 GHz for the specific circuit monitored ranged from 36 to 60 dBm using average upset levels and worst/best numbers for upset levels and effective areas determined from LPC data. This is only for the digital circuits. The duty cycle of the sources used in high power testing meant that the average power was too low (except possibly at maximum power density) to upset any analog circuits, i.e., trip redundancy management monitors which watch analog circuits for problems. The actual system upset level might be lower than predicted above since every possible upset location wasn't tested (16 channels were available to monitor the 180,000 possible upset sites in the three DFCC boxes). How much lower wouldn't be known until the HP tests were accomplished.

**HP**

The microwave sources available in the test chamber covered the frequency band from 1 to 4 GHz. Due to time and resource limitations in the anechoic chamber only two frequencies could be fully evaluated. The first frequency tested was 1.3 GHz, based on the strong coupling and resonance data from LPC and DI tests. The second frequency was 2.8 GHz, picked because of another dip in the upset power level curves. At 1.3 GHz the pulse width was varied between 150 ns and 4.5 us with pulse rate varying from single shot to 150 Hz. The pulse width at 2.8 GHz was 2 us with a maximum 350 Hz repetition rate. Evaluations of two, and three boxes simultaneously illuminated were accomplished. The boxes were illuminated from the front and also from the side. Peak field levels ranged from 0.5 W/cm^2 to 400 W/cm^2. Only digital upsets were expected due to the low duty cycle of the magnetrons; however, there was a chance of analog upset at higher power levels, pulse widths, and repetition rates.

Figure 4 presents minimum peak power upset levels at both frequencies tested for both analog and digital circuits. The figure represents the results of 230 separate test runs. The upset threshold was roughly 10 W/cm^2 at 1.3 GHz, rising to 25 W/cm^2 at 2.8 GHz. The upset threshold was determined at the peak power level which produced a DFCC upset 80% of the time a pulse is applied. The determined upset levels were about 5 dB lower than predicted. We attribute this to the upset site being different than the sites monitored, an almost expected outcome.

All upsets observed except one were digital. The microwave pulse caused loss of cognizant computing by upsetting one, or more, logic locations. The threshold for
between was certain for the pulse widths tested during HP, 150 ns no upset/always U set for the first pulse was fairly narrow, on pulse width was seen as long as the pulse carried enough width down to 30 ns and below would still cause upset). This energy in the digital circuit bandwidth to cause upset. This at the system level, but this is out of scope for this paper. As computer level. There were some pulse rate implications at No dependence on repetition rate was seen at the com-
puter level. There were some pulse rate implications at the system level, but this is out of scope for this paper. As mentioned above, once above a peak power threshold the im-
curred above 10 W/cm² in a narrow frequency range centered at 1.3 GHz. This "bucket" of vulnerability was due to box resonance effects and internal circuit layout. The energy came into the box through the front panel I/O cables, then coupled onto internal DFCC wiring. The vulnerability levels increased on either side of the bucket. No upsets could be induced above 4.3 GHz by directly injecting microwave energy into circuits, simulating external fields above 600 W/cm². This lack of response for frequencies above 4.3 GHz leads us to conclude that this type of DFCC is, for all practical purposes, immune to microwave radiation for frequencies above this.

The upsets in high power tests were due to disruption of digital processing. Cognizant processing immediately halted in the processors effected, indicating the faults were affecting processor operation directly, not the data being processed. The lack of analog upsets were due to the low duty cycle of the microwave pulses. The processor upsets were a function of the peak power of the microwave signal. Once above the peak power upset threshold at a particular carrier frequency, upset occurred within two pulses, almost always on the first pulse. Simple shielding techniques recovered 10 dB of hardness without a great weight and resource penalty.

What This Means For DFCCs In General

These tests imply that the most important variables determining upset potential for DFCC due to microwave EMI are carrier frequency and peak power. Frequency determines best coupling into the DFCC box (probably at a box resonant peak). Peak power is important since the microwave pulse widths and rise times are comparable to the type of signals normally processed by digital circuits. The digital circuit will "see" the envelope of the microwave signal, not just its time average. Average power calculations will generate misleading upset level predictions. When calculating upset power levels one must account for the frequency content of the interfering signal as well as

This is probably due to the combination of shielded twisted-pair cable and protocol of these busses.

At the end of the HP testing, simple shielding techniques were tried to evaluate their microwave vulnerability reduction potential. Normal MIL-STD-461C solutions to this type of upset were used. Backshell connectors and a length of overbraid were added to each wire bundle entering a DFCC. The overbraid were 4 ft in length, roughly 6 wavelengths at 1.3 GHz. As shown in Figure 4, this simplistic shielding added nearly 10 dB of protection to the system, raising the upset level to a minimum of 90 W/cm². The cost? 10 lb, $150 in hardware, and an hour of a technician's time.

CONCLUSIONS

Recap of DFCC Test Results.

The unprotected DFCC was vulnerable to microwave energy simulating radar pulses at field levels above 10 W/cm² in a narrow frequency range centered at 1.3 GHz. This "bucket" of vulnerability was due to box resonance effects and internal circuit layout. The energy came into the box through the front panel I/O cables, then coupled onto internal DFCC wiring. The vulnerability levels increased on either side of the bucket. No upsets could be induced above 4.3 GHz by directly injecting microwave energy into circuits, simulating external fields above 600 W/cm². This lack of response for frequencies above 4.3 GHz leads us to conclude that this type of DFCC is, for all practical purposes, immune to microwave radiation for frequencies above this.

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the frequency response of the target circuits to determine upset possibilities (strictly speaking, the upset potential is driven by the convolution of the detected microwave signal, \( m(t) \), with the circuit natural response, \( h(t) \)).

The tests imply that upsets for complex computer systems are clock cycle independent. Upsets occurred for the first pulse after a peak power threshold was reached, not for any specific repetition rate. This was due to the sheer number of circuits active at any particular time, both clocked (with numerous clock rates) and unclocked, and the pulse widths lasting for at least three clock cycles for the narrowest microwave pulses. Clock rate effects may be difficult to observe for another reason, the microwave generators cannot be pulsed at clock rates of digital computers. Some clock rate effects on analog signal sampling circuits have been seen, but those would occur at much higher microwave signal levels than are in the current environment[2].

Adding simple shielding increased hardness roughly 10 dB over the microwave frequencies where the internal electronics could effectively react. The shielding was nothing exotic, and shows the potential for installing significant protection at small costs.

Future technologies will make the digital computers even harder to microwave upset. This seems contrary to common sense. Even with faster, smaller digital circuits, which at first glance might seem to increase vulnerability, the digital computer construction techniques may mitigate any inherent device vulnerability. Digital data busses, proven hard to microwave effects, will increasingly be used to communicate with formerly analog equipment [6]. Smaller internal circuits will have decreased effective antenna aperture area to capture the microwaves. Probably the most significant hardening will come from the techniques that have to be used to protect the computer (and other onboard avionics) against its own emissions. High speed, high density digital computer boards demand transmission line circuit board design techniques which, by their very nature, eliminate external field coupling. Just due to the fact that the high speed computers can generate significant EMI to other equipment, shielding to reduce this will preclude external EMI influence [6,7].

During the DFCC tests numerous observations were made on upset types, sites and hardening suggestions. The specific upset trends and lessons learned during these tests will be the topic of a future paper.

REFERENCES

References 3 - 6 have not been publicly released. They may be obtained by writing to the author.
7. Conversations with Brad Cope, Shawn Donley, of the Naval Air Warfare Center, Flight Controls Division.