Reconfigurable Electronics for Adaptive RF Systems

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Abstract—This paper overviews the Defense Advanced Research Projects Agency (DARPA) Adaptive RF Technologies (ART) and Arrays at Commercial Timescales (ACT) programs. These programs seek to create adaptable and reusable RF hardware in order to lower nonrecurring engineering development costs and timelines for RF systems and to allow RF hardware to be adapted to new missions after fielding. To achieve this vision, new RF architectures more amenable to reconfigurability have been developed along with component technologies that reduce the performance penalty associated with adaptive RF hardware.

Index Terms—Phased arrays, reconfigurable architectures, microwave circuits, filters, switches, antennas, RF FPGA.

I. INTRODUCTION

Reconfigurable digital circuits, notably the field programmable gate array (FPGA), have revolutionized defense electronic systems by offering improved processing performance compared to general purpose processors but without the large nonrecurring engineering (NRE) costs and development times associated with application specific integrated circuits (ASICs). The flexibility offered by digital FPGAs is especially important in reducing the cost and development time of the low volume, high mix applications encountered by the US Department of Defense (DoD).

In a DoD radio frequency (RF) system, it is very common to have a highly customized RF interface with precisely tuned antennas, filters, up/down converters, oscillators, and other electronics for translating electromagnetic signals into a highly flexible digital backend. As a result, rapid innovation is achievable in the digital portion of an RF system (e.g. waveforms) within the limits of the RF interface. Meanwhile, innovations of the RF interface, including the frequency, bandwidth, number of bands, and efficiency, occur at a much slower pace. In phased array RF systems, the precisely engineered RF manifolds also limit rapid upgrades to the array size and number of steered RF beams. This slow pace in RF analog innovation is particularly problematic in next generation communications arrays where network throughput performance improves by adding additional beams and where many different array sizes are needed to accommodate the wide variety of platforms.

The DARPA ART and ACT programs are creating new, highly integrated architectures and components to realize RF systems that can be reused across many applications and reconfigured in the field.

II. ADAPTIVE AND REUSABLE PHASED ARRAY ANTENNA TECHNOLOGIES

The DARPA ACT program seeks to bring the advantages of reconfigurability and hardware reuse to phased array antenna systems [1]. It does so by encapsulating much of the functionality of phased arrays, including the radiating elements, receivers, exciters and beamforming, into a reconfigurable common hardware module (CM) (Fig. 1).

This architecture leaves a simplified transmit/receive (T/R) module to be custom designed primarily because power amplifiers require band specific tuning to maintain high efficiency. To facilitate highly reconfigurable beam steering across frequency bands, bandwidths and array sizes, RF manifolds, phase shifters and true time delays are realized in the digital portion of the CM. To enable digital beamforming a highly reconfigurable receiver and exciter is included at every element in the phased array. A

![Figure 1. ACT reconfigurable phased array architecture.](image-url)
A reconfigurable antenna array consisting of a tiled surface of pixelated elements that can be patterned electronically to shape the antenna surface currents and resulting radiation pattern (see Fig. 2) provides frequency, bandwidth and polarization control at the radiating layer.

### III. RECONFIGURABLE ANTENNAS

An example of an ACT configurable antenna developed at Georgia Tech Research Institute (GTRI) and BAE systems is shown in Fig. 3 [2]. The design incorporates >50 quad PHEMT switches directly into the antenna radiating surface to precisely control the current patterns within each element of a phased array. The antenna surface is optimized for a particular center frequency, bandwidth and polarization using a genetic algorithm approach developed by GTRI [3]. Initial results have demonstrated reconfiguration of an individual antenna element from C through X band along with bandwidth and polarization control. Key elements to the antenna design include the high performance of the PHEMT switches, the ability to integrate many switches directly into the radiating layer and the ability to mitigate the losses that would normally be associated with the large number of digital control lines.

### IV. RF FRONT ENDS

One of the major challenges in a reconfigurable phased array or single antenna RF system is the realization of a receiver and exciter than can simultaneously be adapted to many applications while achieving the application specific noise figure, linearity and interference mitigation requirements. Such requirements generally dictate both architecture and component decisions that limit configurability and reuse.

The DARPA ART program has realized the RF equivalent of a digital FPGA (see Fig. 4), where a sea of reconfigurable RF components such as amplifiers, mixers, synthesizers and filters are placed in a reconfigurable switch fabric. Such an architecture allows reconfiguration of both the individual components to specific frequency, bandwidth, noise and linearity requirements and reconfiguration of the transceiver architecture (e.g. super heterodyne, low IF, direct conversion, mixer first) to optimize performance and interference mitigation.

![Figure 4. Notional reconfigurable RF architecture](image)

BAE’s Microwave Array Technology for Reconfigurable Integrated Circuits (MATRICs) chip is an 8x10 mm² reconfigurable RF front-end realized in a 180 nm TowerJazz SiGe-on-SOI BiCMOS process. The MATRICs chip operates from DC to 20 GHz with a tunable instantaneous bandwidth from 10 MHz to 2 GHz. This wide operational bandwidth allows for the chip to be configured to address the requirements of multiple and diverse application spaces. To date, the MATRICs chip has demonstrated performance at a level of 90% or better when compared to six custom designed, fixed RF front-ends that were previously developed for different applications.

The MATRICs architecture and die image are seen in Figs. 5 and 6. The MATRICs chip has three primary sub-units: an RF/baseband block (DC – 6 GHz), a microwave block (10 MHz – 20 GHz) and a configurable frequency generator (providing a clock from 10 MHz – 20 GHz). The RF/baseband block contains harmonic rejection mixer-first filters that allow for tuning of center frequency,
bandwidth, and filter order as illustrated in Fig. 7. The mixers within the microwave and RF/baseband blocks allow for a system in-band IIP3 as high as 16 dBm with a noise figure of 21 dB [5]. For lower noise figure the RF-FPGA can be reconfigured in an LNA first architecture to achieve a NF of 10 dB and an IIP3 of 6 dBm [5]. The on-chip frequency generators have a phase noise of -157 dBc/Hz at a 40 MHz offset from a 5.5 GHz reference [6]. Reference 5 illustrates the performance of these sub-blocks over frequency and configuration.

Phase change switches (PCSs) allow for the high levels of configurability found in digital FPGAs, but with an insertion loss per switch from 0.13-0.25 dB [4, 8]. Vanadium dioxide (VO₂) PCSs from Teledyne have produced a high cutoff frequency, \( F_{co} = \frac{1}{2\pi R_{on} C_{off}} \), of over 45 THz [4]. A high cutoff frequency ensures both low insertion loss and high off-state isolation. These VO₂ switches change from a high resistivity to low resistivity semiconductor at 68 °C. Thus, a heater must keep this volatile switch in an ON state.

Non-volatile, temperature controlled germanium telluride (GeTe) PCSs from Northrup Grumman have an \( F_{co} \) of 12.5 THz [8]. The GeTe PCSs change state by changing the phase of the material from amorphous to polycrystalline resulting in an ON/OFF state resistivity ratio of over \( 10^5 \) [9]. A cross-sectional image of a GeTe switch with a NiCrSi heater is illustrated in Fig. 8 while a diagram of the PCS switching profile is shown in Fig. 9.

In order to change the switch from the off-to-on state, the material is heated via the integrated NiCrSi heater above the crystallization temperature, \( T_{cryst} \), of 190 °C for 1 µs. To return the switch to the amorphous off-state, the GeTe material is heated above the melting temperature, \( T_{melt} \), of 725 °C using a heater pulse short enough to allow the material to rapidly cool, preventing recrystallization.
At 18 GHz, state-of-the-art semiconductor switches only retain 27% (45 nm CMOS SOI) and 19% (GaN) of the RF signal after passing through five switches [12, 13, 14], which limits reconfigurability. PCSs can maintain 85% and 73% of the signal after going through five switches at 1 and 18 GHz respectively (Fig. 10). Such an improvement in loss per switch is needed to extend the frequency range and lower the noise figure of reconfigurable RF circuits.

VI. CONCLUSIONS

Reconfigurable RF circuits are a critical technology for reducing the NRE costs and timeframes of developing low volume, high mix, DoD RF systems. To obtain the desired levels of configurability while maintaining performance comparable to fixed, custom designs, the DARPA ACT and ART programs have developed new RF architectures more amenable to reconfiguration and the RF components required by those architectures.

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