X/Ku-Band SiGe BiCMOS Phased Array Chips with Simultaneous 2- and 4-Beam Capabilities

Dong-Woo Kang, Gabriel M. Rebeiz
Electrical and Computer Engineering
UCSD
San Diego, CA, USA
dwkang@ucsd.edu, rebeiz@ece.ucsd.edu

Kwang-Jin Koh
Technology and Manufacturing Group
Intel Corporation
Hillsboro, OR, USA
kjinkoh@gmail.com

Abstract— This paper presents RFIC phased array receive chips capable of formation 2- and 4- simultaneous beams from the same antenna input with 4-bit amplitude and phase control. The design is based on a SiGe BiCMOS process (Jazz SiGe18Hx) and results in excellent isolation between the different beams. The 2-beam chip results in a gain of 5-6 dB per channel at 14-15 GHz, a noise figure of 10.0 dB, a P1dB of -13 dBm per channel (IIP3 of -6 dBm), and an RMS phase and gain error of < 12° and 1.5 dB, respectively. A gain control of 17 dB is available at each channel. Most important, the on-chip isolation between the channels has been fully characterized and is > 30 dB at 11-15 GHz. The beams can operate over an instantaneous bandwidth of > 1 GHz at any frequency between 11 and 15 GHz, and both beams can be at the same frequency if required. The 4-beam chip is currently being tested and the results will be reported at the conference.

Keywords— SiGe BiCMOS, phased array, phase shifter

I. INTRODUCTION

Phased arrays based on silicon RFICs emerged as a practical solution for phased array back-ends due to their high integration density, yield, and functionality on a single chip [1-3]. Several silicon-based phased arrays with 4, 8 and even 16-elements have been demonstrated at X, Ku and even Q-band frequencies and with excellent uniformity [4-9]. This not only reduces the number of chips to be assembled in the phased array but also simplifies the control routing in large arrays. A phased array design for high performance will therefore use III-V components for low-noise amplification and RF power generation together with silicon RFICs for the back-end functions (phase and gain control, power combining, digital control and processing, etc.).

A natural progression from the early work on phased arrays with transmit- or receive-only capabilities is transmit/receive and multi-beam phased arrays on a single-chip [1]. The multi-beam design presents special challenges since high isolation is typically required between the beams. Also, the beams should be able to operate at different frequencies and with wide bandwidth. As will be seen in this work, this can be implemented using silicon RFICs and with excellent performance.

II. SYSTEM LEVEL AND CIRCUIT DESIGN

Fig. 1 presents the system-level diagram of a multiple-beam phased array chip. The RF port is split into N different paths (N=2-4) and each path contains amplitude and phase control circuitry which determines the location of the corresponding phased-array beam. There are N outputs per chip, one for each beam. The interaction between the different paths (beams) should be ideally zero, and the phase and amplitude setting in one beam cannot affect the performance of the other beams. In the implementation shown in Fig. 1, the beams from antenna 1 are added to the beams from antenna 2 using off-chip power combiners. In the future, and for multiple-input designs, the beam combiners can also be integrated on the silicon RFIC.

The circuit level implementation for the 2-beam chip is shown in Fig.2. Starting from the antenna port, the input LNA/Balun is a cascade design with an inductive load and de-Q resistors for wideband operation and followed by a differential emitter follower stage (VDD= 3.3 V, I=20 mA). The LNA/Balun results in a simulated gain and noise figure of ~ 10 dB and 5.4 dB, respectively, at 14-15 GHz, and with wideband operation. The output signal is then using a short passive transmission-line network to two cascade differential amplifiers to form the power dividing network. A cascade design is chosen so as to result in high isolation between the two channels. These amplifiers also have a 1-bit gain control for 0/-10 dB using current steering, and a low output impedance (25 Ω) so as to drive an all-pass I/Q network. The simulated gain is -6 dB at 14-15 GHz.

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The phase shifter is based on an I/Q vector modulator with 4-bit DAC control. It is a similar design to the work reported in [2], but with an additional 3-bit amplitude control using current steering. Again, inductive loads are used with de-Q resistors for wideband operation. The outputs are passed by a differential common-emitter stage and one part of the output signal is terminated internally by 50 Ω (this results in a 3 dB loss in the signal). The phase shifter consumes 12 mA of current and results in a gain of 5 dB at 14-15 GHz.

The 2-beam array is implemented in the Jazz SBC18XL process with 6 metal layers. This process has 0.18μm SiGe transistors (fT of 155 GHz) and 0.18μm CMOS transistors (fT of 50-60 GHz). A 50 Ω microstrip line is realized with top metal (Metal 6) as a signal line and Metal 4 as a ground plane. Standard Jazz transistor cells and models are used, and a ground metal barrier stack formed from Metal 1 to Metal 6 is employed to reduce substrate coupling between the two channels. Jazz ESD protection diodes were placed at the RF ports (1.6 kV, 1.1 A) and larger ESD diodes are placed on the digital control pots (3 kV, 2 A). Full electromagnetic modeling is done on the inductors and transmission-lines using Sonnet\(^1\). A total of 100 pF de-coupling capacitors are placed on-chip between the VDD and ground to also enhance the isolation between the channels. A microphotograph of the 2-beam chip is shown in Fig. 3.

### III. MEASUREMENT RESULTS

The 2-beam phased array was measured on-chip after a standard probe-tip SOLT calibration. The control inputs applied to the chips are supply voltage, the biases of current mirror of each stage, and data bits (4-bit for amplitude and 4-bit for phase). No calibration is done on the chip.

#### A. S-Parameters

The measured S-parameters for a single channel (channel1) are shown in Fig.4. The input and output ports are well matched and agree well with simulations. The measured gain is 3-5 dB lower than simulated (depending on frequency) and this is currently being investigated. The measured NF agrees well with simulations at 14-15 GHz, but is higher at 11-14 GHz due to the lower channel gain. A 17 dB gain control is achieved per channel (simulations is 20 dB). The rms phase and gain error at < 12° and 1.5 dB, respectively, up to 15 GHz. The measured linearity results in an input P1dB of -13 dBm and an input IIP3 of -6 dBm at maximum gain setting. The linearity is determined by the divider stage/I-Q network junction due to the low impedance of the I-Q network and the current driving

\(^1\) Sonnet, ver. 11.52, Sonnet Software Inc., Syracuse, NY, 1986-2007
capability of the divider stage. Both channels results in identical measured S-parameters and therefore, the S-parameters of Channel 2 are not shown.

**B. On-Chip Isolation Measurements**

The on-chip isolation is measured using S-parameter techniques, and the reverse isolation (S12) is better than -50 dB. An accurate measurement of isolation is obtained by measuring Channel 1 (S21) at a fixed phase setting and changing the phase in Channel 2 from 0 to 337.5° [2, 3]. In the 2-beam array, Channel 2 contains the same signal as Channel 1 due to the input power divider, and any leakage from Channel 2 to Channel 1 at the output (after it passes by the Channel 2 phase shifter) can significantly affect the output.

![Figure 5.](image-url)
amplitude and phase of $S_{21}$. This can be modeled using the vector representation shown in Fig. 5. It can be seen that the coupling between the channels ((b) in Fig. 5) can be obtained from the amplitude and phase error in $S_{21}$ due to the phase change in Channel 2.

The measured $S_{21}$ vs. phase change in Channel 2 is shown in Fig. 5. The coupling results in a peak gain and phase error of +/- 0.2 dB and < 2° and this can be fitted to a coupling vector magnitude of 0.023 (-32.7 dB). The coupling is quite deterministic, and for a certain phase in Channel 2, a phase change of 180° results in a change of ~1°. This is shown in Fig.5.

IV. 2-ANTENNA/4-BEAM PHASED ARRAY CHIP

The design chip can be extended to 4-beams with two antenna inputs as shown in Fig. 6. The output of LNA is fed to four cascode differential amplifiers to form the power dividing network. Each beam from the left antenna is added to a corresponding beam from the right antenna using an on-chip active combiner. The chip is currently being tested and the results reported at the conference.

V. CONCLUSION

Phased array receivers capable of simultaneous 2- and 4-beams are designed in a 0.18-μm SiGe BiCMOS technology. The 2-beam chip results in excellent channel-to-channel isolation using S-parameters tests.

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REFERENCES