ANALOG AUTOMATIC TEST GENERATION
DEVELOPMENT PROGRAM

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ABSTRACT
Avionics systems technology advancement has far outreached our ability to define the testing required to adequately accomplish fault isolation. Between the requirements for digital and analog testing, analog has fallen behind the most. To help achieve better analog testing the Air Force has begun work on a six phase development program. This effort is to define and develop an analog test generation system which works in an automated manner. The present plan calls for development and testing to be complete by 1983.

INTRODUCTION
Advances in integrated circuit technology over the past decade have been paralleled by the increasing complexity of modern electronics systems such as those employed by Air Force weapon systems. Consequently, Air Force maintenance activities are increasingly relying on the use of automated aids for locating system, subsystem, circuit board and component failure. The generation of test programs for analog units has, however, been primarily a manual process. Some methods have recently been developed for generating analog test programs using computer-aided design programs.

While these improvements have helped the test program design process, the fundamental testing problem remains, i.e., what tests should be performed to adequately isolate faults. This question is further complicated by boards where test points are either nonexistent or inaccessible. The attempt to adequately address fault isolation in test programs results in long running, complicated programs relying on input/output stimulus and measurement to identify the actual failed component. Realistically, a group of components (ambiguity group) are identified of which any or all could have failed and requiring replacement of all components in the group. Some groups may contain as many as nine or more components. Since the actual failed part is not identified, all replaced parts must be assumed bad and thrown away. Even if the correct group is identified and the proper repair action taken, the problem of maintenance induced faults arises. That is causing other failures not necessarily related to the original problem by attempting to repair the board. These faults must then be found by the same method as the original fault and repaired.

One can easily see this method of fault isolation and repair is both time consuming and extremely expensive. Therefore, a better technique for fault isolation which identifies the failed part the first time is required.

Present techniques for generating analog test programs rely heavily on the experience, skills and "intuition" of the test design engineer using schematic diagrams and measurement requirements data. Advances into automatic aid for test generation have been made but at present their application is limited. The development of new concepts and workable implementations to generate analog test programs in an automated manner is the object of the Modular Automatic Test Equipment (MATE) Analog Automatic Test Generation Development Program. A further goal is to improve the fault isolation capability of the test programs generated.

MATE ANALOG AUTOMATIC TEST GENERATION DEVELOPMENT PROGRAM
At present there are many efforts underway to define and develop an efficient and economical method of automatically generating test programs for analog assemblies both in industry and DOD. The MATE Analog Automatic Test Generation Program is designed to take full advantage of the work already accomplished while leading the designers to a system which best meets the needs of the Air Force. The program is planned as a six phase effort with multiple parallel contracts for actual system design. The multiple parallel efforts approach was chosen since it is felt the present state-of-the-art is not sufficiently advanced to select only one concept. Therefore, many concepts will be funded and given the chance to mature before a final decision is made on the one best way to automatically generate analog test programs.

The initial phase of the program was the selection and hire of an independent technical advisor (TA) to supplement the Air Force team. Selection of the advisor was made on the best combination of experience/background, unbiased approach, communications ability and availability.
Experience/background was considered the prime factor with the following items being given close scrutiny:

a. Experience with Automatic Test Equipment in general and specifically ATE used to support analog assemblies.

b. Familiarity with ATE software design including system, support and test program software. Additionally, familiarity with analog circuit design and the various methods used to generate analog test program sets both manually and in an automated manner.

c. Knowledge of the mathematical sciences such as nonlinear equations, modeling techniques, matrix manipulation and vector analysis.

In addition to these technical experience factors, an assurance of fair treatment to the system developers was sought. Familiarity with present analog ATG approaches and willingness to allow system designers to rebut technical assessments were evaluated. Clarity of communication and availability were evaluated. As a result of this selection process, a contract was definitized on 14 Aug 78 with Decilog of Melville, New York.

The technical advisor's (Decilog's) tasks will be to help define the requirements of an analog ATG system, prepare a Statement of Work which details the system requirements, establish performance requirements, make recommendations for vendor selection and accomplish a technical assessment of designer progress. In order to assure continuing excellence in TA performance, his contract is written to correspond with the phases of the program with only the present phase being definitized. As each new phase occurs in the program the TA's contract must be renewed. This allows the Air Force an opportunity to retain a good TA and release an inadequate TA.

The program is now in Phase Two. During this phase the TA will assist the Air Force with defining the requirements of the Analog Automatic Test Generation (AATG) system, writing a Statement of Work, preparing and release of a Request for Proposal to the AATG system designers. In addition, a set of criteria will be developed to help measure developer progress. These criteria will be used for the initial vendor source selection and the selection which occurs at the end of each development phase. It is anticipated that the criteria will both give progress visibility to the Air Force and to allow the designers insight into the level of effort required to successfully complete the program.

Source selection of the system developers occurs in Phase Three of this program. The criteria developed in Phase Two will be used as the basis for choosing designers to begin implementation of their approaches. It is initially planned to fund between three and five different designers.

The decision on the actual number of approaches funded will, however, be based on a combination of technical excellence of approach and available funds. Competition between designers is sought, but in no case would an inadequate approach be funded just to have competition. It is also not planned to eliminate a good design approach just because the number of other good approaches exceeds five. Therefore, while three to five approaches is the target number, flexibility exists to expand or reduce the number of approaches funded.

Phase Four is the first phase where system development actually occurs. In this phase the developers will be given one year to start development of their approach. At the end of Phase Four, two to three contractors will be chosen to enter an additional year of development (Phase Five). At the end of Phase Five the one best approach will be chosen to enter Phase Six. Phase Six is of two year duration and should result in a prototype system.

CONCLUSION

The Air Force is now preparing the requirements of an analog automatic test generation system which is planned for release in mid 1979. The overall program objective is to develop a system of computer programs and/or a computer system which will aid in an automated manner the generation of test programs for analog type circuits. It is hoped that the prototype system will be tested and ready for operation by mid 1983.