Abstract—A single flux quantum (SFQ) pulse coincidence detector based on resistively shunted nonhysteretic Josephson junctions was designed and simulated. The coincidence detector generates an SFQ pulse when the delay between the arrival of SFQ pulses at its two inputs is less than the coincidence threshold. Simulations indicate that the minimum coincidence threshold time can be as short as 400 ± 200 fs assuming Josephson junction characteristic voltages of 1 mV, overdamped dynamics and 4.2 K operating temperatures. Circuit architectures exploiting this gate are suggested. Estimates of the effects of thermal noise on resolution are presented indicating the potential for various time domain measurements with sub-picosecond resolution.

I. INTRODUCTION

The high speed properties of Josephson electronics offer unique possibilities for high time resolution metrology such as fast sampling, A-to-D conversion, race arbiting, and time domain reflectometry. In this paper I propose an approach to time interval measurement that is based on a simple circuit consisting of several overdamped Josephson junctions. This circuit uses the picosecond pulses of Josephson junctions in a simple way that can be integrated naturally into a frequency vernier measurement apparatus. A junction with a nonhysteretic resistively shunted current-voltage characteristic can be induced to generate voltage pulses whose time integral is equal to the elementary flux quantum $\Phi_0 = 2.07 \text{ mV-pS}$. In particular, the pulse width from an overdamped Josephson junction with a characteristic voltage $V_C = I_cR_J$ is given by $\Delta t = \Phi_0/R_C$ and can be as short as 2 ps for a junction with a typical $V_C = 1 \text{ mV}$. The short widths of SFQ pulses combined with the high plasma frequencies possible with overdamped junctions can be exploited in a simple circuit that detects pulse coincidence from two inputs and has a coincidence threshold that can be as short as several hundred femtoseconds for junction $I_cR_J$ products around 1 mV.

In the next section of this paper I describe the coincidence detection circuit operation, including the results of simulations estimating the potential performance characteristics. The effects of thermal fluctuations on resolution will be discussed. In Section III a time interval measurement system is described, based on the frequency vernier interpolation method. Using conventional electronics, the vernier method has attained time interval resolution limits of about 20 ps. Our simulations show in principle that a carefully designed frequency vernier using SFQ pulses can access time resolutions well below 1 ps at 4.2 K. The reasonable margins and modest numbers of matched Josephson junctions required for this circuit, as well as the intrinsically overdamped dynamics of high-Tc Josephson junctions also make this a feasible application area for high temperature superconductors.

II. PULSE COINCIDENCE DETECTION

Circuit Operation

A nonhysteretic resistively shunted Josephson (RSJ) junction biased just under its critical current can be induced to generate an SFQ voltage pulse (with a concomitant phase slip of $2 \pi$) when triggered by an input pulse. Figure 1 shows a pulse coincidence detection circuit that exploits this effect. Junctions J1 and J2 are input buffer junctions. If they receive pulses of sufficient magnitude at their inputs, they then phase slip and generate pulses, which are routed to J3. IB3 can be adjusted so that a single incoming pulse will be insufficient to cause J3 to phase slip and generate an SFQ pulse. If pulses from J1 and J2 overlap in time, then the sum of the voltage pulses will be large enough to cause J3 to pulse. The coincidence window (denoted $\delta$) is defined as the maximum delay separating pulses from J1 and J2 that will result in triggering J3. The coincidence window is a function of the bias current into J3. As IB3 approaches J3's critical current, $\delta$ increases and the resolution $1/\delta$ decreases. Too high a bias current allows a single isolated pulse from either J1 or J2 to trigger J3 and coincidence events can not be detected. Under the proper bias conditions, a pulse output from J3 indicates the arrival of pulses at the inputs J1 and J2 that were separated in time by not more than $\delta$.

Figure 2 is the simulated operation range of the coincidence detector showing the region where J3 operates correctly as a function of bias current and delay between pulses in J1 and J2. For IB3 around 270 pA, only pulses arriving within 400 fs of each other (neglecting noise) will trigger J3. The following analysis shows that the resolution depends on the value of the $I_cR_J$ product of the junctions and the thermal noise.

Thermal Noise in SFQ Pulser

In this section I estimate the effect of thermal fluctuations on the temporal resolution of the pulse coincidence detector. In addition to the dc bias currents and input pulses, at finite temperatures there will be Johnson noise currents due to the circuit resistances. A fair approximation to the noise currents
is to assume a Gaussian probability distribution for the noise currents with a standard deviation determined by a relevant averaging time that is related to some high frequency cutoff intrinsic to the system. White Gaussian current noise averaged over a time interval $\tau$ will have a probability distribution given by

$$P(\bar{I}_w) = \frac{1}{\sqrt{2\pi}\sigma_{I_w}} \exp \left( -\frac{\bar{I}_w^2}{2\sigma_{I_w}^2} \right),$$

where

$$\sigma_{I_w}^2 = \frac{2k_B T}{R \tau}. \tag{2}$$

The switching properties of J3 are determined by the total effective bias current, including that part of the noise that does not average to 0 over the duration of the input pulses. Thus the relevant time scale $\tau$ is determined by the SFQ pulse widths. This will be given approximately by the larger of either $\Phi_0/4\pi R_N$, L/R, or the RC time constant of the layout. In the following analysis I will assume that the L/R and RC time constants are shorter than $\Phi_0/4\pi R_N$. The physical picture of the overdamped dynamics is that the junction pulses exhibit only small amounts of ringing and overshoot due to parasitic reactance. The junction sees an effective bias current equal to the applied current plus noise currents that are varying over time scales longer than the pulse width. Thus the noise bandwidth cutoff is determined by the SFQ pulse width. The effects of thermal noise on performance can be analyzed using our estimate of the magnitudes of the noise currents and their bandwidths. Substituting $\tau = \Phi_0/2e R_N$ into (2) I get

$$\sigma_j^2 = \frac{2k_B T}{\Phi_0} I_c. \tag{3}$$

I can use this model to determine the critical currents and junction resistances that minimize the coincidence window.

The RMS current noise, $\sigma_I$, is proportional to $I_c^{1/2}$. The intrinsic resolution, that is, 1/$\delta$ or the width of the curve in Fig. 2, ignoring fluctuations, is proportional to $I_c R_N$ because the pulse widths are inversely proportional to $I_c R_N$, where $R_{\text{eff}}$ is the total resistance seen by junctions J1 and J2. $R_{\text{eff}}$ is maximized when R1 and R2 are matched to the $R_N$'s of J1 and J2. To maximize resolution we want the highest possible value of $I_c R_N$. For a given type of junction yielding some maximum $I_c R_N$, the critical currents should be as large as possible to minimize the ratio of noise currents to bias currents, subject to the constraint that the L/R time be shorter than the pulse width. Assuming critical currents and $R_N$ of 250 $\mu$A and 4 $\Omega$ for J1 and J2, and 500 $\mu$A and 2 $\Omega$ for J3, I estimate the standard deviation of the noise currents to be around 5 $\mu$A at 4.2 K and 18 $\mu$A at 50 K.

These relatively large thermal noise currents are a consequence of the high bandwidth imposed by the fast SFQ pulses and translate into a fundamental thermal limitation to the time resolution of this type of sampling circuit. The noise bandwidth questions are of general interest for SFQ digital circuits and may play a role in determining operating margins. Thermally induced bit errors have been reported in SFQ circuits. These were associated with dynamic processes (during pulsing events), consistent with our interpretation of a high noise bandwidth associated with the picosecond scale of the SFQ pulses. Returning to Fig. 2 with an estimate of the thermal noise currents, I estimate that the thermal jitter to the coincidence window will be about 200 fs at 4.2 K and (not shown in figure) 400 fs at 50 K.
High Temperature Operation

This circuit is attractive for high Tc applications even when the large thermal fluctuations are taken into account. At 50 K, a reasonable target operating temperature for high-Tc devices, the Johnson current noise is 18 μA yielding $\delta = 800\pm400$ fs. In contrast to the difficulties involved in fabricating low $T_c$ junctions with high characteristic voltages from low Tc materials, nonhysteretic step edge SNS junctions with $V_{th}$ as high as 1 mV at 50 K have already been reported. Interestingly enough, these junctions may perform better than their low temperature superconducting counterparts at 4.2 K due to their lower parasitic capacitance. Further improvements in junction technology should reduce the minimum $\delta$ and enhance the prospect of high Tc operation.

III APPLICATIONS

SFQ Pulse Width Measurement

SFQ digital circuits offer great promise of extremely high speed with low power dissipation. One factor limiting the ultimate bandwidth of SFQ logic devices is the dispersion and attenuation of the propagating SFQ pulses. The coincidence detector can be used to measure the properties of pulses propagating in transmission lines. I take an approach similar to that described by McDonald et al. but use highly overdamped junctions, which should reduce the complicating interference effects due to plasma oscillations. In this measurement, a test SFQ pulse is split into two identical pulses. One pulse goes into a variable delay, and then both are sent down identical transmission lines (the structure being tested) and fed to a detector junction. The coincidence window analogous to that shown in Fig. 2 is measured as a function of bias current. The observed curve can be used to extract the pulse width and heights. Test structures to perform this type of measurement could be employed in on-chip diagnostics for characterizing pulse propagation in other high speed SFQ circuits.

Time Interval Measurement

The coincidence detector can be used in a natural way in an interpolating time interval measurement system. A block diagram of a frequency vernier interpolater is shown in Fig. 3, and a pulse timing diagram is shown in Fig. 4 to explain the basic operation. The basic idea is to count $N_{total}$ pulses from a master clock that occur between start and stop triggering pulses, then to determine the fractional clock periods, $\Delta t_{start}$ and $\Delta t_{stop}$, that were missed at the beginning and end of the counting interval. The vernier interpolation scheme is a method for expanding $\Delta t_{start}$ and $\Delta t_{stop}$ by a known factor into much longer intervals that can be counted conveniently.

Assume that a time interval is delimited by a start and a stop pulse. The master clock at frequency $F_0$ is kept in a free running state. An external start pulse arrives, clock CL1 is triggered and begins pulsing at frequency $F_0(1+1/N)$, and counters C0 and C1 begin counting pulses from CL0 and CL1. Because clock CL1 has a slightly different frequency than the master clock CL0, the phase delay between pulses from the two clocks shifts with each pulse. After a certain amount of time, determined by the initial phase difference between the two clocks, both CL0 and CL1 pulse coincidentally and coincidence detector D1 will generate a pulse, stopping counter C1.

The count latched into C1 is proportional to the initial time delay between the start pulse and the preceding master clock pulse. For example, if the master clock pulses every 100 ps, the triggered clock pulses every 99 ps, and the start pulse comes in 25 ps after a master clock pulse, then with each successive master clock pulse the triggered oscillator pulse will come 1 ps closer to the master clock pulse. After 25 periods (2.5 ns) the two clocks converge and coincidence detector D1 triggers. For these clock rates, the number of pulses counted by C1 between start and coincidence is equal to the time shift in ps between the start pulse and the previous master clock pulse. More generally, $\Delta t_{start} = C1 / ((N+1)F0)$, where $C1$ represents the count stored in counter C1.

![Fig. 3 Block diagram of a frequency Vernier Interpolator. Clock CL0 is the free running master clock running at frequency $F_0$. Clocks CL1 and CL2, running at frequency $F_0(1+1/N)$ are triggered by the start and stop pulses, respectively. The start and stop pulses also enable the counters C0, C1 and C2. Coincidence detectors D1 and D2 disable counters C1 and C2, which time the asynchronous fractional periods at the beginning and end of the timed interval. C0 counts the integral number of master clock pulses occurring between the start and stop pulses.](image)

![Fig. 4 Timing diagram of the pulses used to detect the fractional clock period occurring at the beginning of the timing interval. The start pulse comes in from an outside line, and triggers the start clock CL1, which begins pulsing. Coincidence between CL1 and CL0 causes coincidence detector D1 to pulse.](image)
determined in the same way as $\Delta t_{\text{start}}$, using the stop pulse instead of the start pulse and coincidence detector D2 and counter C2. C0 accumulates the integral number of periods $f_{\text{master}}$ between the start and stop pulses. The total time between the start and stop time is then given by $\Delta t_{\text{stop}}$-$\Delta t_{\text{start}}$ + C0 $f_{\text{master}}$. Using the vernier, all counting is done at the relatively slow frequencies $F_0$ and $F_0(1+1/N)$, yet the accessible time resolution is $1/(N+1)F_0$. The maximum useful value for N is restricted by the resolution and jitter of the coincidence detectors and clocks.

**Optimization and Fabrication Issues**

To maximize the resolution of the system, the jitter in the two clocks must be extremely low. One attractive SFQ compatible approach to low-jitter clocks might employ multimode cavity stabilized oscillators. In this method, a junction biased just below its critical current is coupled to a junction (or are simply reflected) at the other end, and return between the start and stop time is then given by $\Delta t_{\text{stop}}$-$\Delta t_{\text{start}}$ + C0 $f_{\text{master}}$. The total time between the start and stop time is then given by $\Delta t_{\text{stop}}$-$\Delta t_{\text{start}}$ + C0 $f_{\text{master}}$. Using the vernier, all counting is done at the relatively slow frequencies $F_0$ and $F_0(1+1/N)$, yet the accessible time resolution is $1/(N+1)F_0$. The maximum useful value for N is restricted by the resolution and jitter of the coincidence detectors and clocks.

**REFERENCES**


**IV. CONCLUSIONS**

An approach to high resolution time interval measurement based on the technique of frequency vernier interpolation, using SFQ devices, has been described. The necessary components of the frequency vernier appear to be accessible in both low and high temperature material systems. The modest numbers of junctions necessary to implement a vernier interpolator make the circuit an attractive application of SFQ electronics using either high or low Tc material systems. The thermal analysis suggests that the circuit performance using high-Tc junctions at 50 K will still be in the sub-picosecond range, though it will be substantially degraded from the performance at 4.2 K. The potential sub-picosecond resolution using superconducting electronics represents more than an order of magnitude improvement in performance over that attainable with the best semiconductor based circuits. Finally, the analysis of thermal noise in high bandwidth SFQ devices has bearing on the general problem of fixing margins and optimizing SFQ circuits.