Simplified Ohmic and Schottky Contact Formation for Field Effect Transistors Using the Single Layer Integrated Metal Field Effect Transistor (SLIMFET) Process

Gregory C. DeSalvo, Member, IEEE, Tony K. Quach, Christopher A. Bozada, Ross W. Dettmer, Kenichi Nakano, Member, IEEE, James K. Gillespie, G. David Via, John L. Ebel, Member, IEEE, and Charles K. Havasy, Member, IEEE

Abstract — A new III-V semiconductor device fabrication process for GaAs-based field effect transistors (FET) is presented which uses a single lithographic process and metal deposition step to form both the ohmic drain/source contacts and the Schottky gate contact concurrently. This single layer integrated metal FET (SLIMFET) process simplifies the fabrication process by eliminating an additional lithographic step for gate definition, a separate gate metallization step, and thermal annealing for ohmic contact formation. The SLIMFET process requires a metal FET structure which incorporates a compositionally graded In$_x$Ga$_{1-x}$As cap layer to form low resistance, nonalloyed ohmic contacts using standard Schottky metals. The SLIMFET process also uses a Si$_3$N$_4$ mask to provide selective removal of the InGaAs ohmic layers from the gate region prior to metallization without requiring an additional lithographic step. GaAs MESFET devices were fabricated using this new SLIMFET process which achieved DC and RF performance comparable to GaAs MESFET's fabricated by conventional methods.

I. INTRODUCTION

CONVENTIONAL fabrication methods for GaAs-based metal-semiconductor field effect transistors (MESFET) and high electron mobility transistors (HEMT) use separate lithographic and metal deposition steps to form the drain/source ohmic contacts and the gate Schottky contact. New developments in material growth technology have shown that compositionally graded n$^+$In$_x$Ga$_{1-x}$As layers can be grown on top of GaAs MESFET and HEMT structures to allow nonalloyed ohmic contact formation with a lower contact resistance than can be achieved with n$^+$GaAs cap layers alone [1]-[4]. Also, the lower bandgap energy, higher Si doping levels, and negligible Schottky barrier heights achievable with these InGaAs cap layers allow the use of refractory metals to form nonalloyed ohmic contacts [1]-[4]. From these results, it is possible to extend the conventional refractory metallization schemes that are normally used only for Schottky gate formation to provide both the ohmic contact to the drain/source via the InGaAs ohmic cap layer and the Schottky gate contact to the GaAs MESFET, AlGaAs/GaAs HEMT, or AlGaAs/InGaAs pseudomorphic HEMT channel layers. The main obstacle in using a single metal deposition to provide both ohmic and Schottky contacts is the selective removal of the overlying InGaAs cap layers from the gate region prior to metallization. Although an extra lithographic step can be used to selectively remove this InGaAs layer from the gate region before defining the ohmic drain/source and Schottky gate metal patterns, this defeats the advantage of reducing the number of lithographic process steps needed. The SLIMFET process eliminates the need for a two step lithographic process by incorporating Si$_3$N$_4$ as a secondary mask to allow for selective removal of the InGaAs ohmic contact layers from the gate regions prior to metal deposition.

The SLIMFET process offers several advantages which make it a simple and robust manufacturable process. The SLIMFET process is excellent for characterization of material growth variations, as it minimizes process dependent variables such as gate alignment, ohmic contact formation, and gate recessing. Thus, electrical test measurements and device performance become insensitive to minor process variations. The use of nonalloyed ohmic contacts eliminates alloy dependent problems and contact variability normally associated with alloying, and provides for consistent contacts across the wafer surface and from wafer to wafer. Using a selective etch for the gate recess minimizes process variability, as the etchant selectively removes the ohmic contact layers and stops on the MESFET channel or HEMT barrier layer. Thus, selective etching results in a more consistent and uniform gate recess depth across the wafer and from wafer to wafer [5]. Another advantage of the SLIMFET process is the formation of the drain/source ohmic contact regions at the same time as the gate region, which eliminates the critical gate alignment step for optically defined gates (>0.5 μm) and minimizes run to run variability.

II. THE SLIMFET PROCESS

The SLIMFET process requires FET/HEMT device structures which incorporate In$_x$Ga$_{1-x}$As cap layers to provide nonalloyed ohmic contacts using conventional Schottky retractive metallization schemes [2]. For this initial investigation of the SLIMFET process, a simple GaAs MESFET structure was used, which consists of a standard MESFET structure...
The first two process steps in device fabrication are mask alignment key definition and FET device isolation. Device isolation can either be accomplished by etching mesas or performing ion implantation with oxygen. For demonstration purposes only, etched mesas are used here in describing the SLIMFET process. Since these two steps are identical to those used in standard FET processing, they are not described in detail. A schematic diagram showing the basic processing steps of the SLIMFET process is shown in Fig. 2. After alignment key definition and device isolation has been performed, Si$_3$N$_4$ is deposited over the wafer surface [Fig. 2(a)]. A photolithographic step is used to define and open a gate window region in the Si$_3$N$_4$, which is removed using a buffered oxide etch (BOE) solution [Fig. 2(b)]. Then, another lithographic step is used to define both the ohmic drain/source and Schottky gate regions. If the gates are to be formed optically, then a single mask can be used which defines the drain, source, and gate metal openings. Use of this single mask provides automatic gate alignment with the source and drain, and avoids a critical gate alignment by eliminating a second (gate only) lithographic step. If the gates are to be formed using e-beam lithography, a single resist scheme utilizing an e-beam/optical lithographic (EBOL) process that has been previously developed at Wright Laboratory can be used [6], [7]. In either case, a single process step occurs, providing metal lift-off patterns for the drain, source, and gate regions [Fig. 2(c)]. It should be noted that the alignment between the gate window and ohmic masking is not critical, as the gate window opening of the first mask will have larger openings than the gate length opening of the second mask. The gate window only needs to provide a sufficiently large Si$_3$N$_4$ opening to expose the InGaAs cap layers for the gate recess etch. The critical gate length dimension and gate recess etch is defined by the normal gate lithographic step [Fig. 2(c)], and is not defined by the gate window step [Fig. 2(b)].

The next processing step selectively etches away the InGaAs ohmic contact layers directly under the opened gate regions where the Si$_3$N$_4$ has been opened, exposing the GaAs channel for normal Schottky gate formation [Fig. 2(d)]. The citric acid/hydrogen peroxide etchant system is used as the selective etchant to remove the InGaAs layers without etching the GaAs channel [8], [9]. The InGaAs ohmic layers under the drain/source ohmic regions are not etched since the Si$_3$N$_4$ covers and protects these regions from the citric acid/hydrogen peroxide solution. Once the InGaAs layers in the gate region have been removed, the remaining Si$_3$N$_4$ over the drain/source areas which had been protecting these regions is removed using a BOE solution [Fig. 2(e)]. Thus, the InGaAs layers have been selectively removed from the gate region by incorporating a secondary Si$_3$N$_4$ mask, eliminating the need for a two step lithographic process. With all the drain/source/gate regions exposed, a single metal deposition step takes place, using a standard Schottky gate metallization scheme (such as 200 Å Ti and 5800 Å Au) [Fig. 2(f)]. Finally, metal lift-off is performed, leaving a completed FET device structure with Schottky gate contacts and ohmic drain/source contacts that do not require annealing [Fig. 2(g)]. The remaining Si$_3$N$_4$ can be left on as a passivation layer or can be removed without affecting the FET structure. Also, the single layer ohmic/gate metallization can be used for the interconnect metal of MMIC circuits, and only requires a second level metal process to finish the capacitors, spiral inductors, and air bridges needed for a complete MMIC circuit fabrication.

![Fig. 1. Schematic diagram of GaAs MESFET device structure with InGaAs ohmic contact layers used to develop the SLIMFET process (not drawn to scale).](image)
Fig. 2. Simplified schematic flow diagram showing the basic processing steps of the SLIMFET process (not drawn to scale): (a) device isolation and Si$_3$N$_4$ deposition; (b) define and open gate window; (c) define and open ohmic drain/source and Schottky gate contacts; (d) gate recess to channel layer; (e) expose drain/source lithographic opening to ohmic layer; (f) single contact metallization; (g) metal lift-off resulting in completed device.

Fig. 3. SEM micrograph showing the single layer (200 Å Ti/5800 Å Au) metallization of the drain, gate, and source regions of a 50-μm wide, two finger, center tapped, 1-μm gate length GaAs MESFET fabricated using the SLIMFET process.

as a selective etch is used in the SLIMFET gate recess process to only remove the InGaAs ohmic contact layers and stop on the GaAs channel. This SLIMFET gate recess step can also be used for HEMT structures where the AlGaAs barrier thickness is controlled during molecular beam epitaxy (MBE) growth and is not etched away during gate recess. This AlGaAs barrier layer provides a very good etch stop layer for selectively removing only the InGaAs ohmic contact layers [8], [9], [18], [19], thus making the process fabrication more reliable and reproducible. RF testing included S-parameter testing from 1–26 GHz, and yielded cutoff frequencies ($f_t$) as high as 15.85 GHz and $f_{max}$ of 51.87 GHz, which are comparable to standard MESFET's fabricated using a conventional process.

IV. CONCLUSION

A new FET device fabrication process has been developed and demonstrated, which allows for a single metallization to form both the ohmic contacts and the Schottky contacts in one processing step. This reduces and simplifies several processing steps, namely a critical gate alignment lithography step, a second metal deposition, and a thermal anneal step for ohmic contacts. The use of an optimized mask set for the SLIMFET process to include a combined ohmic/gate optical mask will provide for easier fabrication and increased wafer yield than obtained from standard mask sets. The SLIMFET
The first GaAs MESFET devices with removal of the InGaAs ohmic contact layer from the gate incorporate etch stop layers (i.e., AlAs or AlGaAs) for accurate performance. This new SLIMFET technologies, especially HEMT and pHEMT devices which for characterization of material growth variations, and provides process minimizes many process dependent variables, allowing the SLIMFET process to simplify fabrication of complete techniques. Further work is now progressing toward developing the SLIMFET process to simplify fabrication of complete monolithic microwave integrated (MMIC) circuits.

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Tony K. Quach received the B.S.E.E. degree in systems electrical engineering from Wright State University, Dayton, OH, in 1988.

Since 1989, he has been involved with the research and development of solid state microwave devices and amplifiers at the Solid State Electronics Directorate at Wright-Patterson Air Force Base.

Christopher A. Bozada was born in September 1961. He received the B.S. degree in chemical engineering from Stanford University, Stanford, CA, the B.S. degree in electrical engineering from the University of Missouri, Columbia, and the M.S. degree in electrical engineering from the University of Dayton, OH, in 1983, 1986, and 1989, respectively.

He has been working at the Solid State Electronics Directorate of Wright Laboratory at Wright-Patterson Air Force Base since 1986. His research interests have included design, fabrication, and test of III-V devices. He is currently the team leader of the Advanced Transistor Project.

Ross W. Dettmer received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, in 1988 under the Air Force ROTC scholarship program.

He was commissioned as a Second Lieutenant in the United States Air Force in May 1988. In the period before receiving his first Air Force assignment, he worked at Philips Semiconductor (formerly Signetics) as a device engineer. He was assigned to the Research Division, Solid State Electronics Directorate of Wright Laboratory at Wright-Patterson Air Force Base, in January of 1989. His current work involves advanced HFET's and high power HBT's.

Kenichi Nakano (M'75) received the B.S. degree in electrical engineering from the University of California at Berkeley, in 1968, and the M.S. degree in electrical engineering and Engineers degree in materials science from the University of Southern California, in 1969 and 1972, respectively.

From 1971 to 1981, he was a R&D engineer at the Rockwell International Science Center, where he worked on III-V compound semiconductor optical devices such as detectors and lasers. From 1981 to 1990, he was a department staff engineer at TRW, where he worked on microwave and millimeter wave devices and IC's. In 1990, he joined Wright Laboratory where he is currently managing in-house research projects on HFETs, HBTs, and lasers. He has published more than 25 papers and received 3 patents on semiconductor materials and devices.

Charles K. Havasy (S'91-M'92) was born in Schenectady, NY, in 1970. He received the B.S. and M.S. degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1991 and 1992, respectively.

In 1991 he was commissioned as a Second Lieutenant in the United States Air Force. Since entering active duty in 1992, he has been at Wright Laboratory, Wright-Patterson Air Force Base, OH, where he was working on high temperature JFET's and low noise pHEMT's. His current research interests include microwave devices, laser diodes, and micro-electromechanical devices.

Lt. Havasy was a Theodore von Kármán Scholar from 1991 to 1992, and is a member of Tau Beta Pi and Eta Kappa Nu.