Simulating Total-Dose and Dose-Rate Effects on Digital Microelectronics Timing Delays Using VHDL

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Abstract

This paper describes a fast timing simulator based on Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) for simulating the timing of digital microelectronics in pre-irradiation, total dose, and dose-rate radiation environments. The goal of this research is the rapid and accurate timing simulation of radiation-hardened microelectronic circuits before, during, and after exposure to ionizing radiation. The results of this research effort were the development of VHDL compatible models capable of rapid and accurate simulation of the effect of radiation on the timing performance of microelectronic circuits. The effects of radiation for total dose at 1 Mrad(Si) and dose rates up to $2 \times 10^7$ rads(Si) per second were modeled for a variety of Separation by Implantation of Oxygen (SIMOX) circuits. In all cases tested, the VHDL simulations ran at least 600 times faster than SPICE while maintaining a timing accuracy to within 15 percent of SPICE values.

I. INTRODUCTION

This paper summarizes a method for accurately simulating the operation and timing performance of radiation-hardened VHSIC and VLSI circuits in a rapid fashion using VHSIC Hardware Description Language (VHDL). The goal of this research is rapid and accurate timing simulation of microelectronic circuits before, during, and after exposure to ionizing radiation. Two issues required consideration and resolution to achieve this goal: accurate simulation of microelectronic circuits prior to irradiation and accurate simulation of the changes in circuit performance caused by radiation.

Presently the tools available for predicting the effect of radiation on microelectronic circuits rely on SPICE running radiation-inclusive models to simulate post-irradiation parameter and performance changes [1,2]. However, modeling complex integrated circuits with SPICE simulations requires large amounts of engineering and computer simulation time. Efficient predictive models of the effect of radiation on complex circuits becomes practical only by using fast microelectronic circuit simulators. The core of this research effort was the development of generic, VHDL compatible, models capable of rapid and accurate timing estimates for simulating the effect of radiation on the performance of microelectronic circuits. The initial goal was for the simulator to run at least two orders of magnitude faster than SPICE while maintaining a timing accuracy to within 15 percent of SPICE values.

This paper reports on the model that was developed to satisfy those requirements. Radiation total dose and dose rates affect operation and timing performance of microelectronic circuits in different ways [3,4]. The effect of total dose at 1 Mrad(Si) and radiation dose rates ranging from $1 \times 10^6$ to $2 \times 10^7$ rads(Si) per second were modeled for a variety of SIMOX circuits. Lower dose rates were evaluated but no circuit timing differences were observed. Timing accuracy of the VHDL simulator for four different test circuits was observed to have a mean error less than 4.5% when compared to SPICE results for pre-radiation, total dose and dose rates under $1 \times 10^7$ rads(Si) per second.

II. APPROACH

The method of simulating microelectronic circuit operation and providing accurate timing estimates required four steps to complete. First, the sources of time delays were calculated for each logic gate using SPICE. These included the internal logic-gate delays, fanout-induced drive delays, differences in output rise and fall times for each gate, and the effect of radiation environments on timing delays caused by changes in the transistor drive and leakage. Second, models that accurately estimate the timing delays, including the effects of radiation, were developed. Third, the models were incorporated into VHDL-useable libraries. Fourth, microelectronic circuits were simulated in the VHDL-based simulator and in SPICE to validate the operation and accuracy of the models used in the VHDL-based simulation. Throughout this research effort the SPICE models used were taken from the Texas Instruments 0.8μm SIMOX fabrication process [5].

A. Logic Gate Time Delay Sources

The first step, accurately modeling the sources of time delay was further divided into a four step process. First, the logic gate input load was obtained. Second, the output drive capability was determined. Third, the gate intrinsic time delay

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was determined. Finally, the effects of radiation on the load, drive, and gate intrinsic time delay were obtained from SPICE simulations.

First, logic gate capacitive input load values for a single minimum feature size CMOS transistor pair in the Texas Instruments (TI) 0.8μm SIMOX fabrication process were determined using SPICE [5]. Values for the input load capacitance were determined, by using SPICE, to measure the delay time for a logic gate to change state when connected to the input of a load gate and also when connected to a fixed-value capacitor.

Second, the rise and fall drive capability, modeled as pull-up and pull-down resistances, were calculated using SPICE data. The drive resistance in combination with the driven load impedance were used to calculate the fanout loading effects on timing by taking the product of the two. The drive capability is represented as an equivalent resistance parameter and is determined by measuring the logic propagation delay time for various loads connected to the output. The load capacitances are known constants that were determined in the first step. The pull-up and pull-down propagation delay times are represented by the simple equations:

\[ t_{p,LH} = R_{p,up} \sum C_i, \quad t_{p,HL} = R_{p,down} \sum C_i \]

where:
- \( t_{p,LH} \) - Propagation Delay Time, Output Going Low-to-High
- \( t_{p,HL} \) - Propagation Delay Time, Output Going High-to-Low
- \( R_{p,up} \) - Effective Pull-Up Drive Resistance
- \( R_{p,down} \) - Effective Pull-Down Drive Resistance
- \( C_i \) - Capacitance of the \( i \)th Load

Since pull-up and pull-down propagation delay times are considered separately, independent values for \( R_{p,up} \) and \( R_{p,down} \) were developed.

\( R_{p,up} \) and \( R_{p,down} \) were calculated by measuring the different pull-up and pull-down propagation delay times when a logic gate output was connected to differing numbers of inverter loads in configurations representing fanouts from zero to ten. The change in the pull-up and pull-down propagation delay time, as measured in SPICE, was compared for each of the ten different fanout loads to the calculated pull-up and pull-down propagation delay time using the equations:

\[ R_{p,up} = \frac{(t_{p,LH} - t_{p,LH}^{i=0})}{C_{load}} \]

\[ R_{p,down} = \frac{(t_{p,HL} - t_{p,HL}^{i=0})}{C_{load}} \]

where:
- \( t_{p,LH} \) - Propagation Delay Time, Output Going Low-to-High, Fanout = i
- \( t_{p,HL} \) - Propagation Delay Time, Output Going High-to-Low, Fanout = i
- \( C_{load} \) - Load Capacitance

The output resistances \( R_{p,up} \) and \( R_{p,down} \) were observed to be within three percent of being a constant value for loads from zero to a ten inverter gate load. Assuming a constant value, \( R_{p,up} \) and \( R_{p,down} \) were calculated using equations 3:

\[ R_{p,up} = \frac{(t_{p,LH} - t_{p,LH}^{i=0})}{10 \times C_{load}} \]

\[ R_{p,down} = \frac{(t_{p,HL} - t_{p,HL}^{i=0})}{10 \times C_{load}} \]

The pull-up and pull-down drive resistance terms are easy to calculate once the measurement circuits are setup for each of the logic gates. The drive resistance values in conjunction with the load capacitance combine to make up two of the three terms required to model a logic gate total propagation delay time.

The third and last parameter determined in the pre-radiation time delay model was the internal intrinsic delay of the logic gate. The total delay time of a logic gate is given by the equation:

\[ t_{IL} = t_{p,LH} + t_{int,LH} + t_{p,HL} + t_{int,HL} \]

where:
- \( t_{IL} \) - Total Gate Delay Time
- \( t_{p,LH} \) - Propagation Delay Time, Output Going Low-to-High
- \( t_{p,HL} \) - Propagation Delay Time, Output Going High-to-Low
- \( t_{int,LH} \) - Internal Intrinsic Gate Delay Time, Output Going Low-to-High
- \( t_{int,HL} \) - Internal Intrinsic Gate Delay Time, Output Going High-to-Low

yields the internal intrinsic delay time used to calculate the intrinsic delay parameter.

Since each gate already has a pull-up and pull-down resistive drive capability, the intrinsic delay was represented by a capacitance value given by the equation:

\[ C_{p,up} = \frac{R_{p,up} \times t_{int,LH}}{t_{p,LH} \times C_{load}} \]

\[ C_{p,down} = \frac{R_{p,down} \times t_{int,HL}}{t_{p,HL} \times C_{load}} \]

where:
- \( C_{p,up} \) - Internal Intrinsic Pull-Up Capacitance
- \( C_{p,down} \) - Internal Intrinsic Pull-Down Capacitance

Fourth, radiation effects were added after the models were developed for the nominal operating environment. The effect of radiation on circuit timing was modeled by developing equations, using SPICE data for each of the individual logic gates, where the values of effective drive resistance \( R_{p,up} \) and \( R_{p,down} \) and intrinsic time delay capacitance \( C_{p,up} \) and \( C_{p,down} \) which define the timing characteristics of each gate, were changed by the effect of radiation.

The total ionizing dose radiation-inclusive SPICE models included data for the 1 Mrad(Si) dose level. Thus, the models developed include only this level of total dose modeling.
SPICE simulations were rerun for all the tests used to develop the values obtained for the first five equations and the net effect on the logic gates was to increase the effective drive resistance and intrinsic delay time, while the input load values remained constant. The effective delta drive resistance was calculated for each logic gate using the equations:

\[
\Delta R_{\text{pull-up}} = R_{\text{pull-up}} \frac{\Delta t(10)_{\text{pull-up}} - \Delta t(1)_{\text{pull-up}}}{10 \times C_{\text{load}}} - R_{\text{pull-up}}
\]

\[
\Delta R_{\text{pull-down}} = R_{\text{pull-down}} \frac{\Delta t(10)_{\text{pull-down}} - \Delta t(1)_{\text{pull-down}}}{10 \times C_{\text{load}}} - R_{\text{pull-down}}
\]

where:
- \(\Delta R_{\text{pull-up}}\) - Delta Pull-up Drive Resistance, Post-Rad
- \(t(10)_{\text{pull-up}}\) - Propagation Delay Time Rise, Post-Rad, Fanout = 10
- \(t(1)_{\text{pull-up}}\) - Propagation Delay Time Rise, Post-Rad, Fanout = 1
- \(\Delta R_{\text{pull-down}}\) - Delta Pull-down Drive Resistance, Post-Rad
- \(t(10)_{\text{pull-down}}\) - Propagation Delay Time Fall, Post-Rad, Fanout = 10
- \(t(1)_{\text{pull-down}}\) - Propagation Delay Time Fall, Post-Rad, Fanout = 1

Thus, the pull-up drive resistance used in calculating timing delays for the total dose environment is the sum of \(\Delta R_{\text{pull-up}}\) and \(\Delta R_{\text{pull-down}}\).

The next step was to calculate the model values for the intrinsic time delay capacitance. The effective delta capacitance was calculated for all the logic gates using the equations:

\[
\Delta C_{\text{pull-up-int}} = C_{\text{pull-up-int}} \frac{\Delta t_{\text{LH}}}{\Delta R_{\text{pull-up}} + R_{\text{pull-up}}} (C_{\text{load}} - C_{\text{pull-up-int}})
\]

\[
\Delta C_{\text{pull-down-int}} = C_{\text{pull-down-int}} \frac{\Delta t_{\text{LHL}}}{\Delta R_{\text{pull-down}} + R_{\text{pull-down}}} (C_{\text{load}} - C_{\text{pull-down-int}})
\]

where:
- \(\Delta C_{\text{pull-up-int}}\) - Delta Intrinsic Delay Rise Capacitance, Post-Rad
- \(C_{\text{pull-up-int}}\) - Intrinsic Delay Rise Capacitance, Post-Rad
- \(\Delta C_{\text{pull-down-int}}\) - Delta Intrinsic Delay Fall Capacitance, Post-Rad
- \(C_{\text{pull-down-int}}\) - Intrinsic Delay Fall Capacitance, Post-Rad

After the models were completed for the pre-radiation and 1 Mrad (Si) total dose data, the dose rate data was collected in SPICE. Based on the SPICE modeling results, data collection for the rest of the logic cells was accomplished for the dose rates of \(1 \times 10^9\), \(1 \times 10^{10}\), \(1 \times 10^{11}\), \(1 \times 10^{12}\), and \(2 \times 10^{12}\) rads(Si) per second. The coefficients for drive resistance and intrinsic time delay capacitance were nonlinear over the range of dose rates modeled in SPICE. By fitting the data to several different types of equations it was determined that a quadratic equation would be adequate with a least-squares error of less than 1.0% for the modeled parameters. The coefficients of the quadratic equation were obtained by a least-squares fit for each parameter in the model (drive resistance and intrinsic time delay capacitance). The equations representing the model parameters for the pull-up or the rising state transition are expressed by the equation:

\[
R_{\text{pull-up-dr}} = R_{\text{pull-up}} + D_R \times R_{\text{pull-up-dr-b}} + D_R^2 \times R_{\text{pull-up-dr-a}}
\]

\[
C_{\text{pull-up-dr}} = C_{\text{pull-up}} + D_R \times C_{\text{pull-up-dr-b}} + D_R^2 \times C_{\text{pull-up-dr-a}}
\]

where:
- \(R_{\text{pull-up}}\) - Pull-up Drive Resistance, Dose Rate Inclusive
- \(D_R\) - Dose Rate
- \(R_{\text{pull-up-dr-b}}\) - Delay Time Rise Coeff., Quadratic Terms "b" and "a" + C_{\text{pull-up-dr-a}}
- \(R_{\text{pull-up-dr-a}}\) - Delay Time Rise Coeff., Quadratic Terms "b" and "a" + C_{\text{pull-up-dr-a}}

The equations representing the model parameters for the pull-down or the falling state transition are expressed using similar equations, where pull-up and rise are replaced with pull-down and fall, respectively.

B. VHDL Timing Delay Model

Once all the parameter data were collected, they had to be assembled into models which could be placed into VHDL. A simple equation was used to calculate the time delay through a logic gate. The gate intrinsic time delay capacitance is summed along with all the load capacitors and then multiplied by the pull-up or pull-down drive resistance value to determine the overall logic gate time delay as shown in the equations:

\[
t_{\text{LH}} = R_{\text{pull-up}} \left( \sum_{i=1}^{n} C_i \right) + C_{\text{pull-up-int}}
\]

\[
t_{\text{LHL}} = R_{\text{pull-down}} \left( \sum_{i=1}^{n} C_i \right) + C_{\text{pull-down-int}}
\]

The effects of radiation were incorporated through procedure calls that modified the values of \(R_{\text{pull-up}}\), \(R_{\text{pull-down}}\), \(C_{\text{pull-up-int}}\), and \(C_{\text{pull-down-int}}\) before the circuit simulation is started.

C. VHDL Library Generation

Once the timing models were complete, VHDL descriptions were developed for each digital gate modeled in the SPICE library. Each description contains the code necessary to simulate both the logic function and timing performance of each gate. Data to develop the timing models were recorded from SPICE signal timing data on each individual gate. Simulation of circuits using the models in VHDL was accomplished for two different VHDL models. Both the standard library "base VHDL" which does not contain the detailed timing models for drive, load, and fanout effects and radiation-inclusive VHDL models developed in this research were run to identify the effect of the radiation-inclusive models on run-time and timing accuracy.
D. VHDL Performance Validation

Finally, the SPICE and VHDL methods were compared for speed and timing accuracy. The SPICE simulations were run in HSPICE compiled code to run as quickly and efficiently as possible [6]. The VHDL simulations were run in the Synopsys VHDL Debugger which runs VHDL descriptions in an interpreted model [7]. The advantage of this choice is SPICE, the CPU intensive simulator, was running efficiently using compiled computer code, while the "fast" event driven simulator, VHDL, was running in a "slower" interpreted mode. Thus, the reported run times are conservative and better simulation speed-up ratios would be observed for compiled VHDL for either the standard model or the radiation-inclusive model.

III. RESULTS

The function and timing models were initially simulated in a four-bit full-adder. A four-bit adder was selected for the range of fanout drive and the well understood structure to assist in any debugging required in the radiation-inclusive VHDL models. The initial results indicated the VHDL models would exceed the original goals of simulating a circuit two orders of magnitude faster than SPICE results while retaining timing accuracy to within 15 percent of the SPICE values. Figure 1 and 2 show the logic diagrams for the full adder and the four-bit adder used for the simulation. Note, the VHDL simulations were all conducted by simulating the circuit operation using basic logic gates, NANDs, NORs, inverters, etc.

The next step was to select additional circuits to simulate, in order to validate the accuracy and run time performance of the radiation-inclusive model VHDL across a range of circuit applications and complexities. Three additional circuits selected included a Binary Coded Decimal (BCD) to seven-segment converter, a microwave oven controller, and a 16-bit microprocessor control unit containing over 2800 transistors. The adder as well as the BCD to seven-segment converter are composed entirely of combinatorial logic elements, while the oven controller and microprocessor control unit contain latches and flip flops in addition to combinatorial elements.

![Figure 2. Four-Bit Ripple Carry Adder Block Diagram with WIRE Cell.](image)

For each of the circuits simulated, data were collected to include: run time and timing errors observed for base-VHDL, radiation-inclusive model VHDL, and SPICE simulations for each of the four circuits. The mean of the absolute value of the error (μ) for each logic signal state transition time delay was calculated using the equation:

\[ \mu = \frac{1}{n} \sum_{i=1}^{n} |\Delta t(i)_{VHDL} - \Delta t(i)_{SPICE}| \]  

(10)

where:
- \( n \) - Number of Signal Transitions Measured in Each Circuit
- \( \Delta t_{VHDL} \) - VHDL Time Delay of the \( i \)th Signal Transition
- \( \Delta t_{SPICE} \) - SPICE Time Delay of the \( i \)th Signal Transition

The standard deviation (σ) of the timing error absolute values was also calculated for each circuit using the equation:

\[ \sigma = \sqrt{\frac{1}{(n-1)} \sum_{i=1}^{n} [(\Delta t(i)_{VHDL} - \Delta t(i)_{SPICE}) - \mu]^2} \]  

(11)

Analysis was initially completed on data collected for the four-bit adder. A sample of six of the eighteen signals recorded for the timing results in the four-bit adder are shown in Table 1. Simulation of the radiation-inclusive VHDL model, four-bit adder demonstrated a dramatic improvement in timing accuracy calculation over the base-VHDL results, but with a run time penalty. The radiation-inclusive VHDL model ran two to three times slower than the base-VHDL. The initial results of testing the timing models, incorporated into VHDL descriptions and simulated as a four-bit full-adder, indicated that the timing models would meet the indicated goals of simulating a circuit two orders of magnitude faster while retaining timing accuracy to within ten to 15 percent of the results obtained using SPICE.

Timing error and standard deviation were calculated using Equations (10) and (11). The timing error results for the 18
Table 1. Sample Data for the Four-Bit Full-Adder Including both Base and Radiation-Inclusive Model VHDL.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dose</th>
<th>SPICE (ns)</th>
<th>Base VHDL (ns)</th>
<th>Error</th>
<th>Rad Inclusive Model VHDL (ns)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1rSUM1f</td>
<td>pre-rad</td>
<td>1.0018</td>
<td>1.078</td>
<td>7.6%</td>
<td>0.9960</td>
<td>-0.6%</td>
</tr>
<tr>
<td></td>
<td>1 Mrad</td>
<td>1.0761</td>
<td>1.0790</td>
<td>0.3%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1rSUM1r</td>
<td>pre-rad</td>
<td>1.1213</td>
<td>1.052</td>
<td>-6.2%</td>
<td>1.1030</td>
<td>-1.6%</td>
</tr>
<tr>
<td></td>
<td>1 Mrad</td>
<td>1.2170</td>
<td>1.1900</td>
<td>-2.2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1rSUM4f</td>
<td>pre-rad</td>
<td>2.7040</td>
<td>2.126</td>
<td>-21.4%</td>
<td>2.7260</td>
<td>0.8%</td>
</tr>
<tr>
<td></td>
<td>1 Mrad</td>
<td>2.9402</td>
<td>2.9730</td>
<td>1.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1rSUM4r</td>
<td>pre-rad</td>
<td>3.0756</td>
<td>2.030</td>
<td>-34.0%</td>
<td>3.0570</td>
<td>-0.6%</td>
</tr>
<tr>
<td></td>
<td>1 Mrad</td>
<td>3.2977</td>
<td>3.2260</td>
<td>-2.2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1rCAR4r</td>
<td>pre-rad</td>
<td>2.2742</td>
<td>1.556</td>
<td>-31.6%</td>
<td>2.3310</td>
<td>2.5%</td>
</tr>
<tr>
<td></td>
<td>1 Mrad</td>
<td>2.4980</td>
<td>2.5540</td>
<td>2.2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1rCAR4f</td>
<td>pre-rad</td>
<td>2.6070</td>
<td>1.430</td>
<td>-45.1%</td>
<td>2.6540</td>
<td>1.8%</td>
</tr>
<tr>
<td></td>
<td>1 Mrad</td>
<td>2.7782</td>
<td>2.7820</td>
<td>0.1%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

different time delay signals of the four-bit full-adder are shown in Figure 3. Each simulator run time is represented using a logarithmic scale on the x-axis, while the timing accuracy error is shown using a linear scale on the y-axis, where the bullet denotes the mean (μ) and the bars denote the standard deviation (σ). All simulation run times shown for the base VHDL, radiation-inclusive model VHDL, and SPICE are the average run time for a single simulation. Both the pre-radiation and 1 Mrad(Si) total dose results are shown for the radiation-inclusive model VHDL. Because the four-bit adder contained only three different logic gates, additional testing was required with more complex circuits.

The second combinatorial logic circuit tested was the BCD to seven-segment converter circuit. This circuit is a more diverse and complex circuit than the four-bit full-adder. Testing the radiation-inclusive model VHDL simulator required additional data collection to accurately characterize timing accuracy. A total of 24 different time delay signal transitions were recorded during SPICE and VHDL simulation runs.

The summary results of the time delay error measurements for the BCD to seven segment converter are shown in Figure 4. The simulation run times for each simulator were considerably longer than the run times observed for the adder circuit, due to increased complexity of the BCD to seven segment circuit. Each SPICE simulation took an average of 940 seconds to run, while the radiation-inclusive VHDL simulation took 1.9 seconds to run, and base-VHDL simulation ran in 1.1 seconds.

The microwave oven controller circuit added two different state machine devices and tri-state inverters over the combinatorial logic circuits and, thus, was the first complex
circuit tested with state machine logic devices. The radiation-inclusive model VHDL simulator timing error and standard deviation were calculated using Equations (10) and (11).

The mean ($\mu$) and standard deviation ($\sigma$) of the time delay error measurements for the microwave oven controller are shown in Figure 5. The simulation run times for each simulator were considerably longer than the run times observed for either of the previous circuits because of the increased circuit complexity. Each SPICE simulation pass took 10,800 seconds (3 hours) to run, while the radiation-inclusive VHDL simulation took 5 seconds to run, and each base-VHDL simulation ran in 1.8 seconds.

![Figure 5. Microwave Oven Controller, Simulation Timing Errors.](image)

Timing accuracy for the radiation-inclusive model VHDL simulating the 16-bit microprocessor control unit was 96.4 percent, while the mean error remaining under 4.5 percent for all four circuits. Timing accuracy of the base-VHDL varied greatly, depending on individual signal paths. Since the time delay for each logic gate in the base-VHDL was fixed, any variance in fanout loading led to large errors in the time delay estimates. While the radiation-inclusive model VHDL required more CPU time to simulate than the base-VHDL, it was orders of magnitude faster than SPICE. The radiation-inclusive model VHDL provided timing estimates that were within a few percent of the values obtained from SPICE.

For each of the four circuits evaluated, both the overall time delay accuracy and simulator run time measurements are tabulated and summarized in Table 2. The difference value percentages are the mean of the absolute value of the timing difference for the two VHDL model simulations, using the SPICE results as the baseline. The values shown for the radiation-inclusive VHDL models include the results for both the pre-irradiation, 1 Mrad(Si) total dose, and post-irradiation, dose rates up to and including $1 \times 10^{14}$ rads(Si) per second. The run times for the "base VHDL", radiation inclusive VHDL, and SPICE simulations for four different logic circuits are shown indicating the vastly faster run time for both types of VHDL simulation models run. The "base VHDL" models which are the fastest, use standard VHDL models for timing estimates which do not incorporate the effects of drive, load, and fanout inclusive timing models developed in this research, therefore the base model VHDL simulations run about twice as fast as the radiation-inclusive model VHDL. In all cases, both models in VHDL run two or more orders of magnitude faster than the SPICE.
Table 2. Simulation Run Time and Timing Error Summary

<table>
<thead>
<tr>
<th></th>
<th>Base VHDL</th>
<th>Rad Model VHDL</th>
<th>VHDL Dose Rates</th>
<th>SPICE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Run Time (s)</td>
<td>Diff. (%)</td>
<td>Run Time (s)</td>
<td>Pre.Rad Diff. (%)</td>
</tr>
<tr>
<td>Four-Bit Adder</td>
<td>0.25</td>
<td>29.7</td>
<td>0.9</td>
<td>2.3</td>
</tr>
<tr>
<td>BCD to 7-Seg</td>
<td>1.1</td>
<td>19.8</td>
<td>1.9</td>
<td>4.1</td>
</tr>
<tr>
<td>Oven Controller</td>
<td>1.8</td>
<td>15.3</td>
<td>5.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Microprocessor</td>
<td>15</td>
<td>17.6</td>
<td>32</td>
<td>2.4</td>
</tr>
</tbody>
</table>

The simulator timing accuracy errors are also tabulated and summarized in Table 2. Note, the timing errors for the base model VHDL are worse than the values obtained using the radiation-inclusive VHDL models. The radiation-inclusive model VHDL, which includes timing effects of drive, load, fanout, and radiation effects, provided timing estimate accuracy that compares favorably with the results obtained using SPICE. In the pre-irradiation environment, the absolute value of the mean difference was 4.1 percent or less while the 1 Mrad(Si) total dose simulations yielded a mean difference of 3.8 percent or less. The dose-rate-simulation timing estimates were very similar for dose rates of 1x10^11 rads(Si) per second and lower. Accuracy above 1x10^11 rads(Si) per second deteriorated due to inadequate drive current from the various logic gates. In Table 2, the "base VHDL" shows the timing error for standard model VHDL without the incorporation of the specialized timing models developed for this research.

The radiation-inclusive model VHDL simulator is an accurate timing simulator with the absolute value of the mean difference from SPICE of 4.4 percent or better for all circuits simulated at dose rates of 1x10^11 rads(Si) per second and lower. The radiation-inclusive model VHDL is able to simulate VLSI circuits over 100 times faster than SPICE for simple circuits, with the simulation run time ratio improving over SPICE as the circuit becomes more complex. The simulation run time for the four-bit full-adder was over 380 times faster for the radiation-inclusive model VHDL than SPICE. Likewise, the simulation run time for the more complex 16-bit microprocessor circuit was over 6000 times faster than SPICE.

The dose-rate responses were equally interesting. The absolute mean value difference for the radiation-inclusive VHDL models was as accurate as the pre-irradiation and total dose differences for dose rates of 1x10^11 rads(Si) per second and below. A timing-accuracy limitation exists at radiation dose rates above 1x10^11 rads(Si) per second. The logic gate outputs were unable to sink all the generated photocurrents and provide output voltages at the plus and minus supply voltages. At radiation dose-rates greater than 1x10^11 Rads(Si) per second, photocurrent generation was high enough in the turned-off transistors to keep the turned-on transistors from pulling the output voltage all the way to the rail voltage. An example of this phenomena is observed when the BCD to seven-segment converter was simulated at 2x10^12 rads(Si) per second using SPICE. The three-input NAND gate (NA310) only had a voltage swing from 1.97 to 4.90 volts while the two-input NOR gate (NO210) had a voltage swing from 0.19 to 4.06 volts, as shown in Figure 7. Additionally, the radiation-inclusive model VHDL does not include the effects of photocurrent induced power supply voltage sag in the microelectronic circuit voltage rails.

![Figure 7. Logic Gate Voltage Swing at Dose Rate of 2x10^12 Rads(Si) per second.](image)

IV. CONCLUSIONS

The research goal was rapid and accurate timing simulation of radiation-hardened microelectronic circuits before, during, and after exposure to ionizing radiation. The results were the development of radiation-inclusive VHDL models capable of rapid and accurate simulation of the effect of radiation on microelectronic circuit timing performance. The effects of radiation for total dose at 1 Mrad(Si) and dose rates up to 2x10^12 rads(Si) per second were accurately modeled.

Evaluation of the radiation-inclusive model VHDL led to several observations. The radiation-inclusive models developed in this research are simple and easy to modify for specific microelectronic fabrication technologies, including the parameters that model radiation effects on circuits.
The radiation-inclusive model VHDL descriptions can be simplified for implementation as a non-radiation environment timing simulator by simply nulling the radiation-inclusive model calls. The method of calculating time delays, using drive resistance, load capacitance, and intrinsic internal delay time capacitance, all remain the same. Simulation run time of the radiation inclusive model with the radiation model calls nulled will be faster than the radiation-inclusive VHDL models but slower than base VHDL which does not contain the equations necessary to accurately model the circuit time delays.

Two areas of the timing-estimation modeling have been identified that need additional modifications if improved accuracy of the VHDL-based timing simulator is required. First, significant errors were observed in the modeling of multiple pull-up and pull-down input-to-output transitions. For example a timing difference of 10.4% was observed on a multiple pull-up event experienced by a NOR gate during simulation of the BCD to seven-segment converter. Second, differing rise and fall of logic gate outputs times affected logic transition of downstream gates and requires better modeling.

This research effort demonstrated that it is possible to simulate digital microelectronic circuits orders of magnitude faster than SPICE while still maintaining reasonable timing accuracy. Such improvements in simulation speed were maintained with less than 15 percent loss of accuracy for the pre-irradiation condition, and through a post-total dose of 1 Mrad(Si), and ionizing dose rates of $1 \times 10^6$ rads(Si) per second and lower.

V. ACKNOWLEDGEMENTS

We would like to thank Nathan Nowlin (formally with the USAF Phillips Laboratory) and Ron Schrimpf (University of Arizona) for their valuable comments and discussion in making this paper possible. We would like to thank Mark Mohalic (USAF Rome Laboratory) and John Hines (USAF Wright Laboratory) for their insight and help in the formulation of the research.

VI. REFERENCES