Total Dose Response of Transconductance in MOSFETs at Low Temperature

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Abstract

N and p channel MOSFETs from four bulk CMOS technologies and two CMOS/SIMOX technologies were characterized for total dose response up to 1 Mrad(SiO₂) at temperatures from 10K to 120K. The peak transconductance in the linear region increased in n channel devices and decreased in p channel devices for devices with lightly doped drain (LDD) implants. These changes were much larger as the temperature was decreased and were as much as a factor of 50 in p MOSFETs at 10K. The one technology without LDD showed only a minor change in g<sub>m</sub> with dose even at 10K. The changes in transconductance are most likely a result of hole trapping in the spacer oxide affecting the series resistance.

I. INTRODUCTION

There are many applications for microcircuits at temperatures of 100K and below. In some applications, the parts must also operate after exposure to long term ionization (total dose). The irradiation bias conditions and the allowable shifts in critical electrical parameters for the microcircuit transistors depend on the circuit application and can be quite different for analog and digital. In many applications of mixed signal and digital technologies an important parameter is transconductance which can affect speed and output drive. Transconductance, g<sub>m</sub>, is defined as the rate of increase in drain current per unit increase in gate voltage at a fixed source-drain voltage. What is actually measured in a MOSFET is an extrinsic transconductance, g<sub>me</sub>, which may be defined in terms of the mobility dependent intrinsic transconductance, g<sub>mi</sub>, and a series resistance term, r<sub>ds</sub>, which may be appreciable in LDD devices. The relation between g<sub>me</sub> and g<sub>mi</sub> is

\[
\frac{1}{g_{me}} = \frac{1}{g_{mi}} + \frac{1}{r_{ds}}
\]

Degradation of room temperature g<sub>m</sub> from total dose has been studied extensively and is attributed to mobility degradation from increased interface traps. In fact ∆g<sub>m</sub> is often used as a measure of mobility degradation from which the value of ∆N<sub>IT</sub> is extracted [1]. However, in another study of room temperature degradation of g<sub>m</sub> from total dose, it was shown that both ∆N<sub>QT</sub> and ∆N<sub>IT</sub> can modulate the resistivity of the LDD region and hence alter the value of g<sub>m</sub> [2]. Total dose induced ∆g<sub>m</sub> at low temperature has not been widely reported. One study [3] based on in-house fabricated samples, suggests that since few, if any, interface traps are generated at 77K, degradation of g<sub>m</sub> may be a result of trapped positive charge very close to the Si-SiO₂ interface. Another study [4] suggested that the degradation of g<sub>m</sub> in LDD p channel devices was the result of trapped positive charge in the spacer oxide over the LDD region. The depletion of the p type LDD increases its resistivity causing a degradation of g<sub>m</sub> without affecting mobility. They verified the mechanism by removing the LDD and demonstrating a reduction in ∆g<sub>m</sub>.

In this study we show data from four bulk and two SIMOX technologies. The bulk technologies were all modified to some extent for operation at 77K. However, the SIMOX process technologies are room temperature digital processes which were characterized at temperatures down to 10K to determine the changes that would be required to optimize their performance and radiation hardness at low temperature. Three of the bulk and one of the SIMOX processes utilize spacer oxides and LDDs in both n and p channel transistors. The other SIMOX process does not use LDD and we have not determined whether the other.

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1 Formerly with Mission Research Corporation, Albuquerque, NM.
bulk process uses LDD. In all LDD technologies the peak transconductance in the linear region shows an increase in n channel $g_m$ and a decrease in p channel $g_m$, with total dose. These changes increase significantly as the temperature is reduced. The one technology without LDD shows only slight changes in peak $g_m$ even at 10 K. These results strongly suggest that the primary mechanism is a change in series resistance rather than a change in mobility.

II. DESCRIPTION OF EXPERIMENT

The test transistors used in this experiment are shown in Table 1. The bulk CMOS samples were all from a test chip used to evaluate the technologies for analog applications. The transistor size was 50 $\mu$m by 50 $\mu$m which is representative of critical devices requiring low noise. The minimum feature size ranged from 1.25 $\mu$m to 3 $\mu$m and the gate oxide thickness was 225-250 $\AA$. The transistor design used p+ guardbands in n channel devices to minimize ionization induced edge leakage. The SIMOX samples were from two process technologies, one utilizing LDDs and one without. The transistor size for the LDD technology was 3.6 $\mu$m $\times$ 1.0 $\mu$m and the gate oxide thickness was 200 $\AA$. The transistor size for the non-LDD technology was 100 $\mu$m $\times$ 4 $\mu$m and the gate oxide thickness was 200 $\AA$. Body ties to source were used to minimize the "kink" effect in both SIMOX technologies. Also, both SIMOX technologies used partially depleted transistors so that the front gate was not directly coupled to the backgate.

Table 1

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Process Technology</th>
<th>Feature Size (nm)</th>
<th>$L_m$ (nm)</th>
<th>W (nm)</th>
<th>L (nm)</th>
<th>LDD</th>
<th>LDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Bulk n well</td>
<td>1,25</td>
<td>250</td>
<td>50</td>
<td>50</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>B</td>
<td>Bulk p well</td>
<td>1.25</td>
<td>225</td>
<td>50</td>
<td>50</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>C</td>
<td>Bulk p well</td>
<td>3</td>
<td>250</td>
<td>50</td>
<td>50</td>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>D</td>
<td>Bulk p well</td>
<td>1.25</td>
<td>250</td>
<td>50</td>
<td>50</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>E</td>
<td>SIMOX</td>
<td>0.8</td>
<td>200</td>
<td>3.6</td>
<td>1.0</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>F</td>
<td>SIMOX</td>
<td>1.0</td>
<td>200</td>
<td>100</td>
<td>4</td>
<td>N</td>
<td></td>
</tr>
</tbody>
</table>

Measurements were made on the bulk samples at NSWC Crane in a Gammatron 220 Co$^{60}$ irradiator using a custom liquid nitrogen cryostat with a temperature controlled cold finger. The irradiation temperature was varied in the range of 80 K to 120 K. The data reported herein were taken at 80 K. Three sets of transistor pairs were potted in out each package which allowed for irradiation of transistors at several different gate biases in a single package. The irradiation gate bias varied from -4 V to +4 V in 1 V increments. Electrical data consisted of drain current, $I_D$ versus gate voltage, $V_G$, taken from accumulation to inversion in the linear region with a source-drain voltage, $V_{DS}$ of 100 mV. The data were taken with a standard parameter analyzer connected to the test transistors through a low noise switch matrix using miniature coax cable. Current resolution with the test setup was on the order of 1-10 pA.

The SIMOX devices were tested in a Co$^{60}$ source at S-Cubed using a liquid helium dewar with temperature controller. Measurements were made at 10 K, 40 K, and 80 K at gate bias of 0 V and +5 V for n channels and -5 V and 0 V for p channels. The electrical characterization was performed at drain voltages of 0.1 V and 1.0 V.

The test method was the standard in-situ step-stress approach with static dc irradiation bias and pre/post electrical measurements made at logarithmic total dose levels from 10 krad(SiO$_2$) to 1 Mrad(SiO$_2$). All irradiations and electrical measurements were made at temperature. Electrical data were taken within a few seconds after irradiation. No long term or high temperature anneal data were taken.

III. RESULTS

A. Bulk Technologies

Data are presented at a temperature of ~80 K, for $\Delta g_m$ at an irradiation bias condition of -4 V, 0 V, and +4 V on both n and p channel transistors. The data presented cover the extremes of what was observed and provide a basis for suggesting a failure mechanism.

A typical result for an n channel MOSFET is shown in Figure 1. Figure 1a is a plot of log $I_D$ versus $V_G$ for a 250 $\AA$ gate oxide device at 80 K at several dose levels for an irradiation bias of $V_G$ = +4 V. The threshold voltage shift is seen to be on the order of 3.4 V at 700 krad(SiO$_2$). Figure 1b is a plot of $g_m$ ($\Delta I_D/\Delta V_G$) versus $I_D$ for three dose levels. The data are plotted versus $I_D$ rather than $V_G$ so that the shift in threshold voltage is factored out. The peak value of $g_m$ is seen to increase with dose up to 15 percent at 700 krad(SiO$_2$). The value of $g_m$ in the subthreshold region is seen to decrease by as much as 50 percent. However it should be pointed out that the $V_G$ step size was 100 mV which means that only 3 or 4 data points were taken in the subthreshold region. In addition, the dependence of $I_D$ on $V_G$ in subthreshold is exponential with an inverse slope (subthreshold swing) of about 60 mV/decade at 80 K. The repeatability of $V_G$ from preirradiation to postirradiation was probably no better than 100 mV which could account for the observed changes in subthreshold $g_m$. In inversion near peak $g_m$, however, the dependence of $I_D$ on $V_G$ is nearly linear ($V_{DS}$ = 0.1 V) resulting in a much smaller error in $g_m$ for small errors in the repeatability of $V_G$. A typical result for a p channel device is shown in Figure 2. In Figure 2a log $I_D$ versus $V_G$ is shown at several dose levels. Figure 2b is a plot of $g_m$ versus $I_D$ at the same dose levels. In this case the peak $g_m$ is seen to decrease with dose. The maximum degradation of peak $g_m$ is 25 percent at 1 Mrad(SiO$_2$). In the subthreshold region the value of $g_m$ is seen to decrease by 25 percent.
Figure 1a.

Figure 1. IV and $g_m$ characteristics for various doses for $n$ channel bulk devices from Vendor C.

Again the value of $g_m$ in the subthreshold region is less accurate because of the repeatability of $V_G$.

A summary of the results for all four process technologies is given in Table 2 for $n$ channel devices and Table 3 for $p$ channel devices. The data are shown for 1 Mrad(SiO$_2$) at three irradiation gate biases.

B. SIMOX Technologies

For the SIMOX devices the transconductance was measured in both the linear and saturated regions at 10K, 40K, and 80K. Figures 3 and 4 show the linear region transconductance versus drain current normalized to channel width for 10K at various doses for $n$ channel and $p$ channel transistors, respectively, for the LDD process. The changes in both transistor types are very large, with a 20X increase in $n$ channel devices at 1 Mrad(SiO$_2$) and a 50X decrease in $p$ channel devices at 1 Mrad(SiO$_2$). Figure 5 is a plot of the peak $g_m$ versus dose for $n$ and $p$ channel devices measured with $V_{DS}=0.1$ V. Figure 6 shows the change in peak $g_m$ versus dose for $V_{DS}=1$ V. In the saturated region of operation the changes are much smaller.

The results for the non-LDD device are shown in Figure 7 for peak $g_m$ versus dose at 10K for both linear and
Table 2
Change in Peak $g_m$ for nMOS at 80K, 1 Mrad(SiO$_2$)

<table>
<thead>
<tr>
<th>Vendor</th>
<th>$V_G = -4$ V</th>
<th>$V_G = 0$ V</th>
<th>$V_G = +4$ V</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$\Delta g_m$</td>
<td>$\Delta V_{TH}$</td>
<td>$\Delta g_m$</td>
</tr>
<tr>
<td>+10%</td>
<td>-1.56</td>
<td>+10%</td>
<td>-0.72</td>
</tr>
<tr>
<td>B</td>
<td>+10%</td>
<td>-1.96</td>
<td>+15%</td>
</tr>
<tr>
<td>C$^3$</td>
<td>+15%</td>
<td>-1.84</td>
<td>+10%</td>
</tr>
<tr>
<td>D</td>
<td>+8%</td>
<td>-2.07</td>
<td>+5%</td>
</tr>
</tbody>
</table>

$^1$ Dose - 500 krad(SiO$_2$)
$^2$ Edge leakage prevented data analysis
$^3$ Dose - 700 krad(SiO$_2$)

![SOI nMOSFET with LDD W/L = 3.6/1 $V_g = 0, V_d = 5$ during dose](image1)

Figure 3. Change of $g_m$ with Dose for nFET Operation in Linear Region ($V_d=0.1V$) at 10K.

Table 3
Change in Peak $g_m$ for pMOS at 80K, 1 Mrad(SiO$_2$)

<table>
<thead>
<tr>
<th>Vendor</th>
<th>$V_G = -4$ V</th>
<th>$V_G = 0$ V</th>
<th>$V_G = +4$ V</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$\Delta g_m$</td>
<td>$\Delta V_{TH}$</td>
<td>$\Delta g_m$</td>
</tr>
<tr>
<td>0%</td>
<td>-2.36</td>
<td>-8%</td>
<td>-1.09</td>
</tr>
<tr>
<td>B</td>
<td>No Data</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>0%</td>
<td>-2.29</td>
<td>0%</td>
</tr>
<tr>
<td>D</td>
<td>-5%</td>
<td>-2.13</td>
<td>-7%</td>
</tr>
</tbody>
</table>

![SOI nMOSFET with LDD W/L = 3.6/1 $V_g = 0, V_d = 5$ during dose](image2)

Figure 4. Change of $g_m$ with Dose for pFET Operation in Linear Region ($V_d=0.1V$) at 10K.
Figure 5. Peak $g_m$ for $n$MOSFETs and $p$MOSFETs with LDD for Linear ($V_d=0.1$V) Operation vs Dose at 10K.

Figure 6. Peak $g_m$ for $n$MOSFETs and $p$MOSFETs with LDD for Saturation ($V_d=1$V) Operation vs Dose at 10K.

Figure 7. Peak $g_m$ vs Dose for Irradiation at 10K for $n$ channel device with no LDD.

saturated measurements. Very little change in peak $g_m$ occurs even for linear operation. A summary of the results for the SIMOX devices is shown in Table 4. The changes in peak $g_m$ at 40K and 80K are much less than at 10K.

Table 4
Test Results Summary for SIMOX Devices

<table>
<thead>
<tr>
<th>Vendor</th>
<th>$\Delta g_m$ (PEAK) for 1 Mrad, Linear Region $V_{DS}=0.1$V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n$ channel</td>
<td>10K</td>
</tr>
<tr>
<td>E (LDD)</td>
<td>+1000%</td>
</tr>
<tr>
<td>F (Non-LDD)</td>
<td>-15%</td>
</tr>
<tr>
<td>$p$ channel</td>
<td>-</td>
</tr>
<tr>
<td>E (LDD)</td>
<td>-5000%</td>
</tr>
</tbody>
</table>

IV. DISCUSSION

The results of the total dose irradiations on bulk and SIMOX CMOS transistors at low temperature consistently show that in LDD technologies the peak $g_m$ increases in $n$ channel and decreases in $p$ channel devices. The effect is most pronounced in the linear region of operation and increases as the temperature is reduced. In the one $n$ channel non-LDD sample, very little change was observed in peak $g_m$ even at a dose of 1 Mrad(SiO$_2$) measured at $V_{DS}=0.1$ V and at 10K. These results are consistent with the mechanism proposed by Pantelakis, et al. [4]. The change in $g_m$ is a result of trapped positive charge in the spacer oxide affecting the resistivity of the LDD region. In $n$ channels the series resistance decreases because of accumulation of the $n$ type LDD and in $p$ channels the series
resistance increases because of depletion of the p type LDD. The mechanism is illustrated in Figure 8 for a bulk p channel device. Charge trapping in the spacer oxide can be quite large because of its thickness, which is on the order of 1 μm. As the temperature is lowered below 100K carrier freezeout occurs in the LDD region. This phenomenon increases the effect of the trapped holes in the spacer oxide making the changes in $g_{m}$ more pronounced at lower temperature. The decrease in peak $g_{m}$ in the SIMOX p channel device at 10K and 1 Mrad(SiO$_2$) was a factor of 50.

![Spacer Oxide/Gate Oxide](image)

**Figure 8.** Cross section of p channel bulk device showing charge trapping in spacer oxide.

For the non-LDD device very little change was observed in peak $g_{m}$ under any conditions. This implies that the mobility did not degrade significantly which is consistent with the observation that very few, if any, interface states are generated in the gate oxide at low temperature.

**V. SUMMARY**

N and p channel MOSFETs from four bulk CMOS and two CMOS/SIMOX technologies were characterized for total dose response under a variety of irradiation bias conditions at temperatures ranging from 10K-120K. The peak transconductance was extracted from $I_{D}$ versus $V_{G}$ data taken at two drain voltages. The results show that in LDD devices the peak $g_{m}$ increases in n channel and decreases in p channel transistors. The changes in $\Delta g_{m}$ are much greater for linear operation ($V_{D}=0.1$ V) and for decreasing temperatures where carrier freezeout becomes important. The changes in peak $g_{m}$ for SIMOX transistors at 10K, 1 Mrad(SiO$_2$) and $V_{D}=0.1$ V were a 20X increase in n channels and a 50X decrease in p channels. However, in the non-LDD n channel device, the maximum change in $\Delta g_{m}$ was about 10 percent under any condition. These results support the model proposed by Pantelakis, et al. [4] that positive charge trapping in the spacer oxide results in changes in the series resistance and that mobility is only slightly degraded.

**VI. REFERENCES**


