A BIPOLAR MONOLITHIC PREAMPLIFIER FOR HIGH-CAPACITANCE SSC SILICON CALORIMETRY*

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Abstract

This paper describes a preamplifier designed and fabricated specifically to address the requirements of silicon calorimetry for the Superconducting Super Collider (SSC). The topology and its features are discussed in addition to the design methodology employed. The simulated and measured results for noise, power consumption, and speed are presented. Simulated and measured data for radiation damage effects as well as data for post-damage annealing are also presented.

I. INTRODUCTION

The ever-increasing detector sizes necessary for large-volume calorimetry place severe requirements upon the associated interface electronics regardless of the detector media. For silicon calorimetry, the preamplifier must preserve the fast risetime intrinsic to the detector media while simultaneously sinking the large (100 μA) leakage currents expected from the detector after several years of radiation damage during operation. The preamplifier must have a dynamic range from the charge due to a single minimum ionizing particle (MIP), approximately 36,000 electrons, to that of 5000 or more MIPs. In the case of high-capacitance detectors, the associated preamplifier is required to be designed for a variety of conflicting needs. The large detector capacitances (30 pF - 500 pF) present a difficult hurdle to the designer who desires the best possible signal-to-noise ratio. The capacitance also restricts the speed at which charge integration can be performed, a serious problem since SSC events can occur at 16 ns intervals. These two areas of performance can usually be improved for a given detector-preamplifier by simply increasing the current consumption of the preamplifier. The problem with this approach is that, in a large calorimeter like those proposed for the SSC, thousands of preamplifiers will be needed. Obviously, the preamplifier must be designed for low power consumption since small increases are greatly magnified for the overall system.

The most recent work in the area of preamplifiers for silicon calorimetry is a monolithic BiFET preamplifier1 with approximately twice the noise of the ORNL circuit, illustrated in Fig. 1, and approximately five times the power dissipation. Part of the reason for the improved power dissipation of the ORNL circuit is due to the reduced power supply voltages which are in turn made possible by the use of a gated rebalance loop to compensate for the increasing leakage current from radiation damage of the detectors. Others have employed this concept in a continuous-feedback mode, but the gated approach designed and fabricated in a way useful for SSC applications. The gated approach is superior to that of continuous feedback in this application since the rebalance amplifier is completely off for long periods during normal operation and therefore does not dissipate any power; only the capacitance buffer remains active. Detailed schematics of the ORNL design are presented in Figs. 2, 3, and 4.

II. CURRENT FEEDBACK PREAMPLIFIER TOPOLOGY

There is presently a great deal of interest in current feedback topology in the semiconductor industry. Many

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commercial products have been released recently employing this topology for general use, but this is the first of which the authors are aware that has been specifically targeted to employ the topologies' strengths for physics generally, and an SSC subsystem proposal (Silicon Electromagnetic Calorimeter Collaboration) specifically. This is, therefore, a very timely subject. There have also been few, if any, designs and fabrications using the VTC, Inc. processes for physics applications requiring radiation hardness. This is one of the reasons for choosing this particular foundry.

The initial design philosophy of this preamplifier was to develop a circuit for use with a silicon detector of ~100pF capacitance and exhibit a noise of <7500 rms electrons (rms) for a CR-RC peaking time of approximately 50 ns. The rise time was to be <10 ns to allow the use of shorter peaking times if desired. The power dissipation was required to be <10 mW, charge sensitivity was to be approximately 0.2 V/pC, and maximum charge input was to be 17 pC which corresponds to approximately a 3000 MIPS event (more recent developments at ORNL using ±5 V power supplies are capable of greater than 8000 MIPS). The power supply rails were chosen to be ±3.5 V for reduced power dissipation and because the high-frequency bipolar process used had low breakdown voltage (BVCEO < 10V).

The basic current-feedback (CF) topology chosen for this preamplifier development was described by Comlinear Corporation and Kennedy. Current-feedback has many advantages when compared with more traditional topologies such as differential input or grounded source (grounded emitter). The most distinct advantages are short settling time, excellent loop stability at low closed-loop gains, and high bidirectional slew-rate for low static power dissipation. The major drawback is that the input parallel noise (i.e., the equivalent noise current) is significantly larger than either of the other topologies by approximately the beta of the input device.

A general understanding of current-feedback can be obtained by reference to the electrical schematic of Fig. 2. Transistors Q8, Q11-Q13, and Q16, along with resistor R13 represent a constant-current source for the entire circuit. Current-mirrored transistors Q3 and Q19 define the currents for Q27 and Q28, which in turn define collector currents of Q29 and Q30 via emitter-base ratios. In the standard CF topology, the load resistors for Q29 and Q30 (R7 and R8) are Wilson current mirrors, which replicate IC29 and IC30 to the dominant node for the circuit, at the collectors of Q6 and Q21. Thus in a standard CF circuit, the input error current at the inverting input (equal to IE30-IE29) is equal to the current at the dominant node, which is available to charge the dominant node capacitance and, therefore, to define slew-rate. In this circuit (Fig. 2), we chose to use load resistors (R7 and R8) at the collectors of Q29 and Q30 to replace the normal Wilson current mirrors to provide additional current gain to the dominant pole, much larger voltage gain for the first stage and, therefore, lower overall input noise than with the standard CF topology.

Fig. 2 Current Feedback Amplifier Schematic
The inverting input for CF circuits offers a very low input resistance whereas the noninverting input has a reasonably large input resistance. As seen in Fig. 2, when looking into the inverting input, one sees $r_{en} = 100 \Omega$ or essentially $130 \Omega$ with $I_{C29} = I_{C30} = 100 \mu A$. The paralleled Q29-Q30 inputs also means that the series noise is determined by the parallel series noise of Q29-Q30; in the actual circuit this amounts to less than $100 \Omega$ input equivalent noise resistance. The primary advantage of this very low inverting-input resistance is that it is in parallel with the detector capacitance, thereby offering the capability of using quite large detectors (high capacitance) without seriously degrading the loop transmission (i.e., the loop gain) for the amplifier, since the time-constant $r_{in}C_{det}$ is much less than with either a differential or a cascode input network. This translates into a more stable high-frequency amplifier, with a much enhanced gain-bandwidth product. Conversely, since Q29-Q30 in Fig. 2 are common-base stages with a current gain of only $\alpha = 1.0$, then the parallel input noise (i.e., the equivalent noise current) is much larger than that for other types of preamplifiers, being determined not only by the shot-noise of the base currents of Q29 and Q30 but also by base current noise of Q6-Q7 and Q21-Q22 as well as the thermal noise current of R7 and R8. Fortunately, for the short shaping times necessary for the SSC, the increased current noise should be acceptable.

III. REBALANCE LOOP

One of the design goals of this project was to allow the detector to be directly coupled to the preamplifier, thus precluding the need for a bulky external coupling capacitor. The current flowing from the detector into the input and, subsequently, the feedback resistor of the preamplifier, shifts the dc bias point of the preamplifier as the detector current increases with progressive detector radiation damage. The shift in bias point causes two problems. The first and most apparent is that the output of the preamplifier moves closer to the negative supply rail (see Fig. 1). This reduces the output signal amplitude and, therefore, the dynamic range that can be processed prior to overload (the lower supply voltages required for low power dissipation only compound this problem). The second and less obvious, is that as bias point changes, the preamplifier gain changes because of the nonlinear nature of the transistors, resistors, and capacitors comprising the circuit, an effect normally described as differential nonlinearity. One desirable feature of a preamplifier would be to provide a method of restoring the dc operating point with minimal effect upon the impulse response, noise, or power of the circuit. The circuit shown in Fig. 1 employs a gated rebalance amplifier (error amp) that samples the output for $10 \mu s$ to $50 \mu s$ every $40 ms$ and restores the preamplifier output to a value equal to the bandgap reference voltage which allows the preamplifier to continue to operate within its optimum range of performance despite increases in detector leakage current. The particular implementation shown in Fig. 3 will correct for up to $25 \mu A$ of detector leakage current. The error amplifier of Fig. 3 is basically a gated transconductance amplifier, with a low leakage unity-gain buffer added. A 'HIGH' (+3.5 V) input at the "REBAL IN" terminal will bias Q32-Q33 into an active linear mode, thereby biasing Q49 and Q37 as well. The error voltage stored on the hold capacitor is that required to restore $V_{OUT}$ of the preamplifier to +1.6 V, the dc reference value of the bandgap reference (Fig. 4). This approach could be adapted for much greater leakages by varying the design and the operating parameters. The performance parameters stated above are typical only for this particular design.
IV. IRRADIATION TESTING OF DEVICES

After evaluation of the circuit requirements, we chose to fabricate the overall circuit by using the VTC, Inc. high-frequency bipolar process. The VTC VJ900 npn transistors have a maximum gain-bandwidth product, $f_{T_{\text{max}}}$, of $\sim 6$ GHz, while ppns have $f_{T_{\text{max}}}$ $\sim 1.5$ GHz. Some of the devices available in the VTC VJ900 arrays were available on a separate chip that could be used for pre-design testing. The chips were used for two types of testing: SPICE model confirmation and radiation effects SPICE model correction. The non-irradiated chips were characterized for dc parameters using the Hewlett-Packard Model 4145B Semiconductor Parameter Analyzer and were generally found to be within quoted SPICE parameters. The chips were then irradiated with 1, 2, and 5 Mrads of $^{60}$Co Gamma rays at a rate of 40 krad/hr and retested. From these data, new SPICE models were obtained to more accurately describe the process after irradiation, and thus allow modelling and design of a robust chip. The measurements of $h_{FE}$ vs. $I_C$ are presented in Figs. 5, 6, and 7 for 1, 2, and 5 Mrad $^{60}$Co. Table 1 presents the Early voltage measurements for non-irradiated devices and for 5 Mrad irradiation.

**Fig. 5** VTC TLN1 Beta vs. Collector Current for 0 Mrad to 5 Mrad

**Fig. 6** VTC T6NW Beta vs. Collector Current for 0 Mrad to 5 Mrad

**Fig. 7** VTC TVPA35 Beta vs. Collector Current for 0 Mrad to 5 Mrad
Table I
VTC Early Voltage Measurements With Gamma Dose

<table>
<thead>
<tr>
<th>Type</th>
<th>Dose Mrad</th>
<th>Ic (µA)</th>
<th>VA (V)</th>
<th>VA % Diff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLN1</td>
<td>0</td>
<td>4.9</td>
<td>26.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>4</td>
<td>17.5</td>
<td>-33.0</td>
</tr>
<tr>
<td>TLN1</td>
<td>0</td>
<td>22.5</td>
<td>29</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>23</td>
<td>23.9</td>
<td>-17.6</td>
</tr>
<tr>
<td>TGNW</td>
<td>0</td>
<td>67</td>
<td>33.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>66</td>
<td>30.1</td>
<td>-9.0</td>
</tr>
<tr>
<td>TVPA35</td>
<td>0</td>
<td>3.5</td>
<td>10.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>2.7</td>
<td>7.6</td>
<td>-28.8</td>
</tr>
</tbody>
</table>

V. RESULTS

The preamplifier speed, noise, and power were measured pre- and post-radiation at 1 and 5 Mrad gamma exposures. The simulated pre-rad risetime was 5 ns and noise was 5975 εrms for 60 ns CR-RC peaking time. The simulated pre-rad power dissipation was 7 mW. After 5 Mrad gamma dose, the simulated risetime was 8 ns, noise was 7187 εrms, and dissipation was 2.3 mW. These values compare favorably to the measured values shown in Table II, except the post-rad risetime was worse than the simulation. The changes in risetime and power dissipation are believed to be due to a shift in the operating point of the biasing circuitry. The reduced power indicated that supply currents had dropped causing the circuit to become 'starved'. The annealing process caused the biasing to return somewhat to normal and, therefore, bring the circuit closer to initial performance. The annealing cycle was tested because collaborations had expressed interest in an annual anneal cycle to repair radiation damage in both detectors and electronics. From the perspective of preamplifier performance, this would appear to be a useful process.

Table II
Results of Tests

<table>
<thead>
<tr>
<th>Condition</th>
<th>Risetime</th>
<th>Power (+/-3.5 V)</th>
<th>ENC (60 ns Peaking)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-rad</td>
<td>6.3 ns</td>
<td>7.5 mW</td>
<td>6300 εrms</td>
</tr>
<tr>
<td>5.3 Mrad</td>
<td>20 ns</td>
<td>2.1 mW</td>
<td>6600 εrms</td>
</tr>
<tr>
<td>5.3 Mrad</td>
<td>9 ns</td>
<td>5 mW</td>
<td>6800 εrms</td>
</tr>
<tr>
<td>4 hrs.</td>
<td>100°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VI. FUTURE WORK

This preamplifier was designed specifically for a detector size of 100 pF. A need for several different detector sizes with capacitances ranging from 30 pF to >400 pF has been subsequently identified. ORNL personnel have designed seven preamplifiers using the HARRIS Semiconductor VHF dielectrically isolated process for use with these detectors. Results from this development will be reported at a later date.

VII. CONCLUSION

A preamplifier designed at ORNL specifically for high-capacitance silicon calorimetry has been described. The pre- and post-radiation performance has been discussed for both the preamplifier devices and the preamplifier itself.

VIII. ACKNOWLEDGEMENTS

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IX. REFERENCES