Radiation Response of Silicon on Diamond (SOD) Devices

N.K. Annamalai, Jon Sawyer, Pramod Karulkar, Witko Maszar, and Maurice Landstrass

Phillips Laboratory (PL/VTIL), Hanscom AFB, MA 01731-2909, USA
Electrical and Computer Engineering, Northeastern University, Boston, MA 02115, USA
MIT Lincoln Laboratory, Lexington, MA 02173-9108, USA
(Present Address: Microelectronics Research Laboratory, 9231 Rumsey Road, Columbia, MD 21045, USA)
Allied Signal Aerospace, Columbia, MD 21045
Crystallume, Menlo Park, CA 94025

ABSTRACT

Field effect transistors are fabricated on two types of Silicon-On-Diamond (SOD) structures and their radiation response is studied. The results are compared with the radiation response of simultaneously fabricated SIMOX devices. The feasibility of fabricating field effect transistors on SOD structure is demonstrated for the first time and the extreme radiation hardness of such a structure is also verified.

I. INTRODUCTION

Silicon-on-diamond\textsuperscript{1,2} (SOD) is a form of silicon-on-insulator (SOI) technology\textsuperscript{2} in which the buried insulator comprises a thin film of diamond. In addition to the generic advantages of SOI, SOD technology offers two major benefits: (1) Good thermal conducting property of diamond makes power dissipation easy and hence it is possible to develop ULTI circuits or power devices with capabilities beyond those achieved by existing technologies. (2) High chemical bond strength (50 kcal/cm\textsuperscript{3}) and high carrier mobility which make diamond very insensitive to radiation, will also make SOD structure extremely radiation hardened. Although more materials work needs to be done to realize usable SOD technology, we summarize here a preliminary investigation of SOD technologies. We conducted a series of experiments to establish the extreme radiation hardness of SOD and the feasibility of fabricating SOD MOSFET devices: (1) characterization of aluminum-CVD diamond film-silicon (MIS) capacitor, (2) characterization of quick turn around (QTA) back channel MISFET's made in an experimental ZMRSOD structure\textsuperscript{1}, and (3) fabrication of conventional, concentric NMOS FET's with polysilicon gates in bond-and-etchback SOD (BESOD). This paper discusses these experiments and establishes the potential of SOD as an extremely radiation hardened material.

II. EXPERIMENT

A. MIS Capacitor:

A CVD diamond film was deposited on a 3" silicon wafer. CVD diamond\textsuperscript{3} was deposited by DC plasma reactor using 5% methane gas at 35 Torr pressure at 725\degree C with a power of 700W\textsuperscript{4}. Thickness of diamond films ranged from 1 micron to 3.7 microns. Aluminum metal dots (4.6x10\textsuperscript{-3} cm\textsuperscript{2}) were deposited on top of the diamond film. The backside of the wafer was metallized for a good substrate contact.

B. ZMRSOD Quick Turn Around QTA Back Channel MISFET's:

Fabrication of the ZMRSOD structure used in this study is illustrated in Figure 1. Polycrystalline, intrinsic diamond films (1000 nm) were deposited on (100), p-type silicon substrate using a well characterized, plasma CVD process. The diamond deposition was done on the wafer leaving a 0.25" rim free of diamond. One micron thick polycrystalline silicon film was deposited on this wafer covering the whole wafer, including the rim area. Using the rim area as the single crystal silicon seed, the polycrystalline silicon was crystallized into a single crystal by a zone melting recrystallization technique.\textsuperscript{5} In the ZMR process, the wafer is held at a temperature very near the melting point of silicon in an inert environment and zone melting recrystallization (ZMR) is achieved by scanning a strip heater in close proximity of the surface of the wafer. Characterization of the SOD structure was done using SEM, Raman Spectroscopy and Scanning Auger Microscopy to verify the integrity of the buried diamond film at two stages in the experiment: (1) after the deposition of the CVD diamond film on silicon wafer and (2) after completing the device fabrication. Fig. 2 shows a cross sectional scanning electron micrograph of a ZMRSOD sample after the device fabrication.

A conventional MOSFET fabrication sequence could not be applied to SOD substrates in the beginning of the work for several reasons: interaction of the CVD diamond film with various VLSI fabrication steps was not understood very well, the possibility of cross contamination of fabrication equipment was a concern, and the warp of the experimental SOD substrate would have interfered with automatic wafer handling. A quick turn around (QTA) back channel MISFET structure (Fig. 3) was devised and fabricated in a CMOS
fabrication facility using a few steps to prove the feasibility of the SOD technology. The fabrication of ZMRSOD QTA back channel MISFETs, which comprised an undoped body and boron doped source and drain regions, provided better understanding of the various fabrication issues and allowed study electrical properties of the SOD material.

During ZMR processing, polysilicon was deposited either directly on the diamond film or on top of a very thin (30 nm) barrier/adhesion layer of deposited SiO2. The QTA back channel fabrication process involved use of RCA cleans, piranha clean, buffered HF dips, downstream oxygen plasma and a wet photoresist stripping solution of tetramethyl ammonium hydroxide. These steps did not have any adverse effect on either the diamond or the silicon film as judged by optical microscopic inspections and profilometer thickness measurements. Diamond films react rapidly with oxygen above 700° C. Hence oxidizing environments could not be used to anneal the source drain implants. A short anneal in oxygen at 900° C in a preliminary experiment not only oxidized all the exposed diamond but caused hundreds of micron deep lateral oxidation of the diamond film under the silicon film. A low temperature anneal cycle was chosen to assure some degree of dopant activation without any risk of sample destruction by decomposition or peel off. The process steps used for fabrication of QTA back channel MISFETs are as follows:  
1. Reduce Si thickness for ease of processing.  
2. Form islands by photolithography and RIE.  
3. Define source, drain and capacitor area in photoresist.  
4. Implant 2x10^15 cm^-2 B^+ at 30 keV and at 30 keV.  
5. Clean and Sinter for 240 minutes at 455° C in N2.

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Electrical testing of QTA involved placing the probe needles directly on top of the source and drain regions (Fig. 3) and measuring the I-V characteristics of the back channel by using the substrate as the back gate. Good contact was obtained by lightly scrubbing the probes on the source and drain areas.

C. BESOD MOSFETs

The sequence of fabrication steps for forming a BESOD substrate can be understood from Fig. 4. Two epitaxial layers were grown on a seed silicon wafer (labelled 1 in Fig. 4): The first layer (labelled 2) was an etch stop layer with a heavy doping of boron and germanium, the second layer (labelled 3) was an undoped silicon layer of desired thickness to fabricate
the field effect transistors. A 1.5 micron thick CVD diamond film, (labelled 4) was deposited on top of the undoped Si epi layer (3). On top of the diamond film (labelled 4), an approximately 10 μm thick polysilicon (labelled 5) was deposited and polished to obtain a smooth surface. A clean, (100) silicon wafer (labelled 6 and called a handle wafer) was bonded to the polysilicon layer. Polishing of polysilicon buffer layer was required for the intimate contact. The roughness of the diamond film made the polysilicon surface very rough and unacceptable for bonding. Wafers were bonded by placing two wafers in intimate contact at 800° C for 10 minutes in N2 ambient.

![Diagram of BESOD structure]

**Figure 4.** Scheme to form BESOD structure.

Most of the seed wafer was removed by grinding the backside. EPW (ethylenediamine-pyrocatechol-water) was used to remove the remaining handle wafer up to the etch stop layer. Another etchant [1 part HF (49%), 3 part HNO3 (70%), and 8 parts CH3COOH] was used to remove the etch stop layer. The residual layer at the end of etch stop layer was removed by a proprietary non-selective etch.

A number of discrete MOSFET's were fabricated in the BESOD silicon film (labelled 3 in Fig. 4). The device structure was concentric in geometry and consisted of a drain area with diameter of 40 μm separated from the source by the gate, having an inside diameter of 40 μm and an outside diameter of 48 μm. For comparison, a few of the SIMOX wafers were concurrently subjected to the same type of processing steps. The following fabrication process was used for BESOD MOSFET's:
1. Mesa formation by photolithography, reactive ion etch and resist removal.
2. RCA clean, 80 nm PECVD oxide deposition, and annealing at 800° C in N2 for 30 min.
3. Deposition of in-situ doped, n-type polysilicon and gate electrode formation by photolithography, reactive ion etch and resist removal.
4. Definition and ion implantation of NMOS source/drain areas.
5. Deposition of 500 nm PECVD oxide and Annealing at 800° C for 30 Min in N2.
6. Contact formation by lithography and RIE etch.
7. Of Al/Si/Cu metallization.
8. Sintering at 425° C for 30 minutes in N2.

**D. Radiation Testing:**

Irradiation's were performed in an ARACOR 10 keV x-ray machine at a dose rate of 140 krad(SiO2)/min. The worst case biases used during the radiation tests are marked in the appropriate figures. Although the doses are quoted in the units of rad(SiO2) for consistency and ease of comparison with conventional SOI, the actual dose delivered to the diamond film will be less than the SiO2 dose because of the lower atomic number of carbon.

**III. RESULTS AND DISCUSSION:**

**A. MIS Capacitor:**

The C-V Characteristics of an MIS diamond film capacitor as a function of the total dose are shown in Figure 5. Considering that the thickness of the diamond dielectric in this structure was 1.5 μm, a shift of -30 V after a total dose of 40 Mrad(SiO2) is very small. The threshold voltage shift in the case of a buried silicon dioxide of the same thickness will be extremely high. The radiation induced flat band shifts observed in this work are larger than those observed in a previous publication which examined very thick diamond films. Although we do not have a satisfactory explanation for this apparent discrepancy, it could simply be related to different thicknesses of diamond films, different applied electric fields, or to an unknown variation in the quality of the diamond.

![Graph of C-V Characteristics]

**Figure 5.** C-V characteristics of an MIS diamond capacitor as a function of total dose, with wafer grounded and aluminum contact held at +5 V during irradiation.
diamond films. The SOD capacitor measurements thus established the inherent radiation hardness of the CVD diamond film. Probably, the high bond strength of diamond does not allow any significant charge trapping. In the previous work\(^8\), the radiation hardness of diamond films has been speculatively related to the high mobility of charge carriers in diamond. Unfortunately, the previous experiments and those discussed in this paper were not designed to identify the origin of the radiation hardness in diamond films. A separate study of the physics and chemistry of the radiation damage in diamond films is required. Interface states between silicon and diamond film also need to be characterized.

The dielectric constant of the diamond films, estimated from the C-V measurements, was found to be 6.7. It is higher than that of natural diamond and might indicate the presence of non-diamond components in the thin film. A careful analysis of the films with very high resistivity is needed to understand the dielectric properties.

![Graph](image-url)

**Figure 6.** Leakage current characteristics of a CVD diamond film on silicon.

The intrinsic diamond film resistivity was also studied as a function of the electric field using MIS structures formed by 0.0046 cm\(^2\) thin film, aluminum dots deposited through a shadow mask directly on a CVD diamond film and also on the diamond film obtained after ZMR processing by etching off the top silicon film. The conductivity of diamond (Fig. 6), which was symmetric in applied voltage, was very uniform over the sample area of over 10 cm\(^2\) indicating that the conductivity was not a result of localized defects. The defects or the structure and composition that made the film less insulating had a uniform distribution over the diamond film. The through current density increased roughly two orders of magnitude after the ZMR processing which involves heating the wafer to temperatures near the melting point of Si.

Decomposition of some of the diamond could occur at such high temperatures. In the case of ZMRSOD with a 30 nm SiO\(_2\) barrier layer under the Si film, the leakage current through the buried dielectric was low enough (nA range) to allow observation of good ZMRSOD back channel MISFET characteristics. On the other hand, the buried diamond insulator in BESOD samples was electrically very leaky and hence BESOD back channel MISFETs could not be tested.

### B. ZMRSOD Back Channel MISFETs

ZMRSOD quick turnaround back channel MISFETs exhibited good I-V characteristics with threshold voltages in the range of 4 to 11 volts, subthreshold slopes in the range of 1200 to 2000 mV/dec and maximum low field p-carrier mobility was 40 cm\(^2\)/V.s. The low threshold voltage is due to the lack of intentional doping of the channel (body) region of the MISFET. The low mobility, which did not vary significantly after irradiation, indicates the presence of interface roughness, impurities, and defects in the experimental ZMRSOD substrates which is not surprising. The subthreshold swing indicates the density of interface states to be of the order of \(10^{11} \text{eV-cm}^{-2}\). The leakage current in the off state is high (nA) because the annealing of the source and drain implant at the low temperature did not form good junctions. Although deleterious and in need of improvement, small back gate leakage (100 pA at \(V_B = 5 \text{ V}\)) did not change upon irradiation and did not interfere with the measurement of the MISFET characteristics.

![Graph](image-url)

**Figure 7.** Subthreshold characteristics of a ZMRSOD QTA back channel MISFET as a function of the total x-ray dose.

Subthreshold characteristics of a ZMRSOD back channel MISFET are shown in Figure 7 as a function of the x-ray dose. The source and drain were grounded during irradiation and
The back gate was biased at +20 volts. The irradiated devices exhibited a threshold shift of less than -10 V. The change in the shape of the characteristic after the high dose (2.78 Mrad(SiO2)) is due to parasitic effects caused by the mesa surfaces. The increase in the off leakage after irradiation is attributed to the deterioration of the front surfaces and the sidewalls of the drain junction.

The threshold voltage shift of -80 V for a total dose of 2.78 Mrad(SiO2) seen in Fig. 7 for a ZMRSOD MISFET. The radiation induced threshold voltage shifts for SIMOX and SOD are compared in Fig. 9 which very clearly indicates the superior radiation resistance of SOD. The most striking feature of the SOD threshold voltage shifts is the reversal in the threshold voltage shift seen above 278 krad(SiO2). Although the origin of this reversal is not clear from the present investigation, we speculate that it is caused by trapping of negative charge in the buried SOD dielectric. The buried dielectric in Figs. 7 and 9 contained a thin (30 nm) layer of SiO2 between the diamond film and the Si film. Only positive charges are trapped in the oxide film and they saturate at higher doses. The diamond film or the oxide-diamond interface probably traps negative charge. The saturation of positive charges and continued trapping of negative charges manifests as the reversal of the radiation induced threshold shift in Fig. 9.

C. BESOD MOSFET’s

Functional NMOSFET’s were found in the BESOD device fabrication experiment. Subthreshold characteristics of front channel NMOSFET’s concurrently fabricated in BESOD and SIMOX substrates are shown as a function of the radiation dose in Figs. 10 and 11 respectively. A worst case bias, which involved applying +5 V to the front gate and grounding the source-drain, was used during irradiation. BESOD front channel appears more radiation hardened than the SIMOX front channel even though they were processed concurrently.

![Figure 8. Subthreshold characteristics of a SIMOX QTA back channel MOSFET as a function of the total x-ray dose, with V_s=V_D=0 V and back gate voltage = +5 V during irradiation.](image)

The front channel subthreshold swing of fully depleted, single implant SIMOX NMOSFET with 190 nm Si film is -375 mV/dec. It is a result of using 80 nm plasma deposited gate oxide and does not truly reflect the good quality of the SIMOX material. NMOSFET’s with nearly ideal subthreshold swings have been fabricated separately in the same SIMOX material using the conventional CMOS fabrication process. The plasma enhanced CVD process, though not optimized as a gate oxide process, was selected only because it was available and could be implemented easily into SOD device fabrication sequence. Low temperature deposition of ULSI gate oxides of better quality than that of the oxides used in this work is now possible. On the other hand, we believe that the quality of the material is mainly responsible for the poor (1970 mV/dec) subthreshold swing of the BESOD MOSFET(Fig. 9). The subthreshold swing is degraded by the following factors: (1) quality of the experimentally prepared BESOD silicon surface, (2) quality of
the thin BESOD silicon film, (3) the quality of the Si-diamond back interface in the fully depleted NMOSFET, and (4) the deposited gate oxide. The experimentally produced BESOD silicon films were relatively very thin (<100 nm).

Figure 10. Subthreshold characteristics of a front channel BESOD NMOSFET as a function of the total x-ray dose.

Figure 11. Subthreshold characteristics of a front channel SIMOX NMOSFET as a function of the total x-ray dose.

The silicon-diamond interface was created during the deposition of diamond on silicon at an elevated temperature. The density of interface states for this interface was not determined because of the high leakage through the diamond film. The back gate (substrate) did not have much of a control in the device performance due to the conductivity of the diamond. This lack of electrical isolation of the Si film from the back side Si substrate might also have contributed to the poor subthreshold swing. As discussed in the ZMR-SOD section and also in Ref. 8, a thin layer of SiO₂ between the BESOD Si film and the diamond film might have helped in improving the I-V curve by improving the diamond-Si film interface. But the interfacial SiO₂ layer was avoided in an attempt to deposit high quality, insulating diamond films directly on Si.

This experiment demonstrated for the first time that it is possible to fabricate BESOD FET's. The buried dielectric radiation hardness, which is inherent to the diamond film, is not experimentally proven for the BESOD case. We hope to accomplish this by first resolving the fabrication issues such as obtaining smooth, electrically insulating diamond films and controlling the quality of Si film and the diamond-Si film interface by using different interfacial layers.

IV. CONCLUSION

Silicon on diamond technology is experimentally evaluated as an alternate radiation hardened device technology. The extreme radiation hardness of CVD diamond films is established by using a MIS capacitor structure and the ZMR-SOD quick turn around (QTA) back channel MISFET structure. The feasibility of fabricating BESOD FET's has been demonstrated for the first time in this work. But the radiation hardness of the buried diamond in the BESOD structure could not be proven due to the excessive electrical conductivity of the buried diamond film. A number of fabrication issues were encountered in this work. However, their detailed discussion is beyond the scope of this paper. It must be acknowledged that the sensitivity of diamond to high temperature processing especially in oxidizing environments does make fabrication of IC's in the generic SOD structure very difficult. But we believe that SOD devices can be realized using modified SOD structures, modified device structures, novel fabrication sequences, and high quality deposited dielectrics. The work described here needs to be continued to optimize diamond films from the point of view of SOD device technology, development of viable SOD substrate and device fabrication technologies, and verification of the tolerance of SOD to radiation as well as high temperatures.

V. ACKNOWLEDGMENTS

Thanks are due to Mr. Mike Batty and D. P. Vu of Kopin Corporation for the ZMR work, the Digital Integrated Circuits Group at Lincoln Laboratory for device fabrication, and Dr. Walter Shedd for the use of Phillips Laboratory radiation facilities.

VI. REFERENCES

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