A GaAs MESFET IC for Optical Multiprocessor Networks

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Abstract—A GaAs, E/D mode, self-aligned, refractory-gate, MESFET process and circuit family has been developed for the integration of fiber-optic data link functions (e.g., photodetection, amplification, clock recovery, and deserialization) on a single chip. This paper describes the process and presents results on integrating a complete optical receiver, including the photodiode and clock recovery circuits, onto one chip. The chip functions use over 2000 devices, and performance at 1-Gbit/s speed, while dissipating less than 300 mW of heat. This chip is the most complex high-performance OEIC reported to date.

I. INTRODUCTION

The interconnection of many processors is a growing theme in the data processing industry [1], [2]. For optical data links to play a role in the interconnection networks of these multiprocessor complexes, a high-performance reliable, compact opto-electronic integrated circuit (OEIC) technology is needed to integrate network functions together on a single semiconductor chip [3]. Typical functions implemented at network interfaces, which would be important to capture on a chip are shown in Fig. 1, and include a mix of digital and analog, and optical and electronic functions, with a chip complexity at the LSI level. With powerful processors at the network nodes, multi-gigabit-per-second speed may be required in this chip (for example, [4]). The distances are likely to be short (less than 1 km) to keep data transit times between the nodes short with respect to the machine instruction cycle time.

This paper describes a GaAs MESFET IC process that has many of the characteristics desired for this application. At this time, it appears that GaAs is the best technology candidate, as other implementations (e.g., based on Si or InP material systems) will be limited to bulky hybrid chip modules, low levels of integration, and yield and reliability concerns due to transistor limitations or complex strained layer epitaxial growth techniques [5], [6].

We also present experimental results on the integration of some key functions onto a single chip, performing at gigabit-per-second data transfer rates. The chip described represents the highest level of integration yet reported in integrated gigabit-per-second opto-electronics chips.

II. MESFET OEIC

Refractory-gate MESFET processes have gained favor for GaAs logic and memory applications because they are simple, provide good thermal stability of device characteristics, and offer potential for the reduction of device parasitic resistance and capacitance [7]. The self-aligned gate MESFET technology employed in fabricating the chip reported here is an enhancement of that described previously by some of the authors [8], with significant changes in lithography and wiring, and the incorporation of gate sidewalls with a moderate implant beneath them. The process employs $^{29}$SiF$_4$ channel and source-drain implants, sputtered WSi$_{2.1}$ refractory gates, Ni-Au-Ge ohmic contacts, Si$_3$N$_4$ and SiO$_2$ insulation, and Ni-Au wiring. A gate length of 1 μm was used in all circuits. The FET channel and photodetector implant was activated by furnace annealing either in an arsenic overpressure or with a Si$_3$N$_4$O cap deposited by plasma-enhanced chemical vapor deposition (PECVD). Furnace annealing of the source-drain implants was carried out with a Si$_3$N$_4$ cap. Following patterning of the gate and detector electrodes, a moderate-dose self-aligned implant was carried out, after which a blanket Si$_3$N$_4$ layer was deposited and etched to leave triangular sidewalls at the edge of the gate. The sidewalls keep the heavy source-drain implant away from the gate edge, resulting in a reduction in gate capacitance and an improvement in breakdown voltage.

The lithography for these circuits, which have 11 masking levels, was carried out entirely by step-and-repeat projection lithography. Positive photoresists were used except for the gate and wiring levels. For these levels, a negative-tone image-reversed structure was used for optimum resolution (for the gate etch), and for retrograde
Fig. 1. Network interface functions. The typical functions required for an interface to a network. For full duplex operation, both sets of functions would be required at each network node. The shaded functions are performed at the bit speed of the serial link and thus require higher performance circuits.

### Table I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Initial</th>
<th>1 hr</th>
<th>2 hrs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 μm p-FET threshold voltage (Vₜ)</td>
<td>0.181</td>
<td>0.190</td>
<td>0.190</td>
</tr>
<tr>
<td>1 μm n-FET threshold voltage (Vₜ)</td>
<td>0.730</td>
<td>0.734</td>
<td>0.730</td>
</tr>
<tr>
<td>1 μm p-FET β factor (β = Vₜ/βₙ)</td>
<td>0.176</td>
<td>0.181</td>
<td>0.181</td>
</tr>
<tr>
<td>1 μm n-FET β factor (β = Vₜ/βₙ)</td>
<td>0.133</td>
<td>0.136</td>
<td>0.136</td>
</tr>
<tr>
<td>1 μm Schottky diode clamping voltage (Vₚ)</td>
<td>0.131</td>
<td>0.290</td>
<td>0.155</td>
</tr>
<tr>
<td>Ohmic contact resistance (Qₚ (%)</td>
<td>325</td>
<td>328</td>
<td>328</td>
</tr>
<tr>
<td>Source-drain sheet resistance (Ω cm)</td>
<td>8.15</td>
<td>6.65</td>
<td>6.75</td>
</tr>
<tr>
<td>Gate metal sheet resistance (Ω cm⁻¹)</td>
<td>0.15</td>
<td>1.22</td>
<td>1.20</td>
</tr>
<tr>
<td>Ohmic metal sheet resistance (Ω cm⁻¹)</td>
<td>0.06</td>
<td>0.09</td>
<td>0.13</td>
</tr>
</tbody>
</table>

The refractory-gate metallurgy, as well as the Ni-Au-Ge process with in-situ sputter clean used here [9], were chosen for their relatively good thermal stability. In order to access the stability of the metallurgy, wafers were tested after completion of the wiring levels, and then again after 1 and 2 h of annealing at 375°C. The results, which are summarized in Table I, suggest that all parameters remain within acceptable limits after annealing. The change in Vₜ of about 30 mV appears related to relaxation of the stress of the dielectric overlayer. FET's oriented at right angles to those reported here show a similar change in the opposite direction. No significant change in Vₜ is observed during the second hour of annealing. The change in ohmic contact resistance for the circuit data shown in Table I was the closest to being unacceptable, and off-line experiments have indicated a way to lower these variations.

### III. FULLY INTEGRATED, SELF-CLOCKED OPTICAL RECEIVER OEIC

We have used the above technology to fabricate a 1-Gbit/s optical receiver containing the photodetector, amplifier, decision and bias control circuits, and clock recovery circuits necessary for an optical data link interface. A photo of this chip is shown in Fig. 2. These circuits have been described separately elsewhere [10], [11], so their performance will only be summarized, pointing out where the above chip devices and processes aided functional performance. This paper is the first report of the combined operation of these functions on a single chip. These functions are the most noise and jitter sensitive functions in the link, as well as being a mix of analog and digital circuits, and therefore are a good testbed of the requirements for an OEIC. The total device count on the chip is ~2500, making it the most complex OEIC chip yet reported. It dissipates ~300 mW of heat.

#### A. Optical Receiver

The receiver schematic is shown in Fig. 3, and consists of an interdigitated, metal-semiconductor-metal.
Schottky-barrier (I-MSM) photodiode, a transimpedance preamplifier, a four-stage, differential cascode-type amplifier, a Schmitt trigger decision circuit, and an automatic bias control circuit for the preamplifier. The IMMSM detector utilizes the WSi gate metal because of its optimal Schottky-barrier height, and to assure a temperature and time stable Schottky barrier for its contact fingers. The enhancement implant of the MESFET process was used under the detector to create a region that prevents surface trapping of photogenerated carriers, and thus prevents tails in the PD pulse response. The resulting dark current is 5 nA, and the measured (by optical picosecond probing technique) optical bandwidth is 14 GHz. The active area of the detector was about $5.5 \times 10^{-5}$ cm$^2$ making it useful with multimode fibers. Low input capacitance to the amplifier is important for high-sensitivity receivers. The IMMSM PD design yields a low PD capacitance of 150 fF, while the ability to integrate the detector close to the preamp yield a parasitic capacitance of < 20 fF. The sensitivity at 1 Gbit/s has been measured to be $-22$ dBm for an NRZ code and $BER < 10^{-9}$. The modeled receiver bandwidth is > 1.5 GHz with a $-24$-dBm sensitivity, so that we expect a packaged chip to operate at over 2-Gbit/s speed.

The receiver circuit was designed to be entirely differential to improve its immunity to power supply noise and reduce its dependence on threshold voltage. This differential design and the use of a tight detector/amplifier coupling, possible only in a fully integrated design, resulted in little noise being coupled into the receiver input from other circuits on the same chip. Differential designs do require more transistors to implement, but a technology
recovered clock output. Horizontal IS
with LSI IC capability means that transistors are a cheap commodity. This abundance of logic circuit capability becomes very important when designing real systems, which often have link monitoring and service functions to perform along with data transmission operations.

B. Clock Recovery

Fig. 3 also shows the schematic of the phase-lock loop (PLL) clock recovery circuit. To make the chip less susceptible to noise, and take advantage of the digital characteristic of these MESFET transistors, digital circuits were utilized in the voltage-controlled ring oscillator (VCO) and the loop filter (a digital filter using up-down counters). Once again, differential circuits were employed in the PLL to prevent signal distortion and improve speed. The rms jitter measured is less than 25 ps at 1.25 Gbit/s, and the locking range was ±10 percent of the bit rate.

C. Fully Integrated Performance

Fig. 4 shows typical operation of both clock and receiver on the same chip. Oscilloscope plot (a) is the 1.25 Gbit/s, $2^7 - 1$ pseudorandom sequence input from a laser illuminating the receiver's photodiode (optical power nominally −16 dBm). Oscilloscope plot (b) illustrates the recovered data output from the receiver, and (c) is the recovered clock. A 1/10-speed "byte clock" output is also available.

An important question associated with the integration of an optical receiver with large amounts of digital logic is the on-chip feedback from the digital circuits to the front end of the amplifier. Fig. 5 indicates the potential of excellent noise immunity arising from complete functional integration on a single chip. Shown in the oscilloscope trace is the receiver's amplifier when no optical input is illuminating the photodiode, taken while the clock on the chip is free-running at the bit speed, and driving a bit speed signal off the chip. On-chip noise would show up as a pattern effect at the output of the amplifier, and such patterns were not measurable.
IV. CONCLUSION

In conclusion, we have described an OEIC process and devices which are attractive to use in link adapters for optical multiprocessor networks. We have demonstrated a fully integrated optical receiver, with clock recovery, which is state of the art for integration complexity in high-speed OEIC chips. As the electronic technology is built on a digital LSI IC base, other digital circuits can be readily integrated onto this chip, and results will be reported elsewhere.

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REFERENCES


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Dr. Crow has received IBM Research Division Outstanding Contribution Awards for work on injection laser arrays for liquid-crystal displays in 1979, and for high-speed fiber-optic link development in 1983. In 1986, he was on the technical program committee of the IEEE Optical Fiber Communication Conference. In 1987, he was appointed to the Photonics Panel of the U.S.-Government's National Research Council.

John F. Ewen (S'80-M'81) was born on November 11, 1955, in Chicago, IL. He received the B.S.E.E., M.S.E.E. and Ph.D. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 1976, 1977, and 1981, respectively. His graduate work dealt with surface acoustic wave devices and nonlinear acoustic wave propagation in lithium niobate and ZnO/Si material systems.

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